

USER GUIDE
ALD-232A
BUS ANALYSIS PROBE
for
RS232D, RS449 and IEEE1284



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1. Introduction

The ALD-232A analysis probe provides state and buffered timing analysis capability for both serial and parallel busses. Fast, easy and reliable connections can be made from the logic analyzer to the RS232, RS449 and the parallel bus with supplied Y-cables. Full duplex data is displayed in state mode.

- Small, attractively styled, and easy setup
- State decoding for IEEE 1284 Compatibility, Nibble, and ECP modes
- State and timing configuration and data formatter files are provided on diskette to simplify logic analyzer setup
- User-friendly mode selection uses a keypad and LCD
- Serial Transfer rates to 230Kbaud
- Simultaneous Display of both State and Timing

1.1 Specifications

- **RS232D(v.24) and RS449 Asynchronous:**

Rates: 50, 75, 110, 150, 300, 600, 1200, 1800,
3600, 4800, 7200, 9600, 19.2K, 38.4K,
57.6K, 115.2K and 230.4K baud

Bits/Char: 5, 6, 7 or 8

Parity: Odd, Even, or None

Stop bits: 1, 1.5, 2

- **RS232D(v.24) and RS449 Synchronous:**

Rates: up to 230.4 K baud

Formats: SDLC and HDLC

Bits/Char: 6 bit transcode, 7 or 8 bit ASCII, 8 bit
EBCDIC

Clock Source: transmit data clock may be
supplied by the DCE or the DTE

- **Required Instrument:**

Any HP or Agilent 165xx or 167xx logic analyzer

- **IEEE 1284:**

Modes: Compatibility (Centronics or AT
parallel), Nibble, and ECP

- **Bus Loading:**

RS232D: 5K ohms @ 20pF on all lines

RS449: 12K ohms @ 20pF on all lines

IEEE1284: 10K ohms @ 20pF on all lines

- **Power Required:**

~325 mA supplied by the Logic analyzer

- **Mechanical:**

4.0" x 7.5" x 2.0" (WxLxH) with 2 POD
connections on right side of unit

- **Signals Supported:**

All primary RS232D/449 signals;

All IEEE1284 signals

- **Skew (Timing Analysis):**

RS449: Less than 200 ns

RS232: Less than 300 ns

- **Connectors:**

Logic Analyzer: 2 (direct to LA cable, no
terminator needed)

RS232D: DB25*

RS449: DB37*

IEEE1284: DB25*

* Both male and female connectors supplied via
a 'Y' cable

1.2 Logic Analyzers supported

All Hewlett-Packard and Agilent analyzers are supported by the ALD-232A except for the 168x and 169x. If you have an early HP analyzer (HP1650, 16510, etc), please contact ALD for an appropriate diskette. Support for the current models of HP or Agilent analyzer (16550, 1660, 1670, 16600, 16700, etc) is included with the enclosed diskette.

1.3 Installing the Software

Two disks are supplied with your ALD-232A. One contains the files needed RS232/RS449 and the other is IEEE1284. The contents of each are:

IEEE1284 Disk:

FILENAME	Description
DISK1.DAT	167xx data formatter installable files
INDEX.TXT	
INFO.TXT	
IAA1284.I	Data Formatter for the 16500
ieee1284._B	16550 Configuration

RS232 Disk:

FILENAME	Description
DISK1.DAT	167xx data formatter installable files
INDEX.TXT	
INFO.TXT	
RS232._B	16550 Configuration for the 16500
IAA232A.I	Data Formatter for the 16500

These disks contain both configuration files and software that formats the logic analyzer screen (a.k.a. an 'inverse assembler'). The method of installation depends upon your logic analyzer.

1.3.1 16500/166x Installation:

Copy the files *rs232._b*, *IAA232A.I*, *IEEE1284._B* and *IAA1284.I* to the location on your hard disk where you keep your configurations (e.g. \\configs). It is often convenient to make separate directories for each, i.e. one for RS232/449 and one for IEEE1284. Keep the diskettes supplied with the ALD-232A in a safe location in case of damage or accidental erasure from the hard disk.

Next, load the configuration file, either *rs232._b* or *IEEE1284._B* into the slot where your 16550 (or equivalent) card is located on your analyzer. DO NOT use "LOAD ALL". This

will result in the error message “SOME OR ALL CONFIGURATIONS NOT LOADED”. Next load the data format utility, either rs232.i or IAA1284.I, as appropriate. After you have saved for the first time, it will not be necessary to load the format utility again.

1.3.2 16700 Installation

The screen format utilities must be ‘installed’ in the 16700 series analyzers. Both the RS232 and IEEE184 disks are ‘installable’ diskettes. Insert the appropriate diskette into the analyzer’s floppy drive and invoke the ‘System Administrator Tools’ and the Software Install tab. Click the *Install* button. In the Media window, select the Flexible disk then click the *Apply* button. Select the package in the window and click the *Install* button. This will install the appropriate data formatter in the logic analyzer and configurations in the case of the RS232 installation.

After you have installed the RS232 diskette, a directory structure will be created on the logic analyzer: */logic/configs/ALD/ALD232A RS232.*

In this directory there will be 5 files:

RS232.__A	16550A Configuration	RS232.__D	16717A Configuration
RS232.__B	16555A Configuration	RS232.__E	16752A Configuration
RS232.__C	16712A Configuration		

Choose the file appropriate to the logic analyzer board in your 167xx.

For the IEEE1284, only the data formatter is installed with the software installation. The 5 configuration files on the diskette must be copied manually. ALD suggests a directory under */logic/configs/ALD/ALD232A IEEE1284* parallel to the *ALD232 RS232* sub directory.

If the analyzer in your 167xx is not one of these types, attempt loading one of the configurations. The logic analyzer will attempt a conversion process. Some warnings may appear. Commonly a pod re-assignment message will identify how the pods on the conversion target should be connected in reference to the original configuration.

If the conversion is not successful, contact Advanced Logical Design, Inc.

1.4 Equipment Supplied

- RS232D, RS449, and IEEE 1284 Bus Analysis Probe
- This User Guide
- Diskette including configuration files and screen data formatter
- 2 flat ribbon 'Y' Cable for connecting to the target bus

1.5 Minimum Equipment Required

In addition to the equipment supplied above, a Hewlett-Packard or Agilent analyzer in the 165x,6x, 7x family or the 165xx is required.

2. Installation

2.1 Initial Inspection

Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until the contents of the shipment have been inspected mechanically and electrically. If the contents are incomplete, if there is mechanical damage or defect, or if the instrument does not operate, notify Advanced Logical design, Inc.. If the shipping container is damaged, or the cushioning materials show signs of stress, notify the carrier as well as the ALD office. Keep the shipping materials for inspection by the carrier.

2.2 Connection to the Logic Analyzer

The ALD-232A both derives its power from the host logic analyzer and provides it data through the pod connection cables. Both pods 1 and 3 should be connected. Pod 1 provides state data and Pod 3 provides timing data. The pod cables from the logic analyzer are plugged directly into the right side of the ALD-232A. No additional terminators or adapters are required.

3. Operation Overview

All operations of the ALD-232A are controlled by the keyboard. When the logic analyzer cables are plugged into the ALD232A, the unit will power up in the mode it was last in. Navigation through the options is very simple. An arrow (->) will point to the item that can be changed. A new value may be selected for that item by scrolling through the choices with the ◀ and the ▶ keys. To move to a different item, use the ▲ and ▼ keys. The item at the top of the screen is the type of analysis desired [RS232 ASYNC, RS232 SYNC, RS449 ASYNC and RS449 SYNC]. The last screen in the sequence is an informational screen.

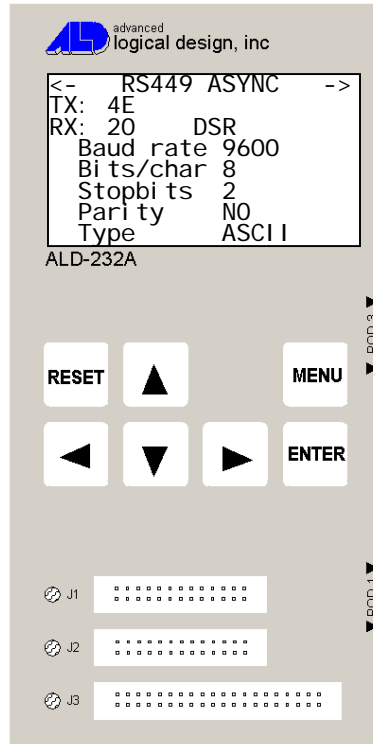


Figure 1: ALD-232A Top Panel

Below each analysis type selection are the adjustable parameters for that selection. These are adjusted as described above. The changes made will take effect immediately. After 10 seconds, the new value will be stored in an internal EEPROM so that they will be available after the next power-on sequence.

The display brightness is adjusted on the informational screen. It is the only user adjustable item on the informational screen.

4. Analyzing RS232D or RS449

Either of these two busses may be observed either in state or timing or both modes simultaneously. In state mode, the ALD-232A will capture the serial data, check it for framing and parity errors and present it to the logic analyzer as a character. Transmit and receive channels are monitored and displayed in 2 separate columns. The logic analyzer screen will also display the state of the control lines (e.g. RTS, CTS, CD, DSR, DTR) at any time a new character is received from either transmit or receive channels.

In timing mode, the signals are displayed and labeled on the logic analyzer. The signals displayed are TTL versions of the bus signals. The buffering introduces some delay and necessarily some skew, but this is less than 7% (MAX) of a bit time at 230.4K bits per sec.

Load the appropriate configuration file from the [/logic/configs/ALD/ALD232A_RS232](#).

4.1 Introduction

The RS232D/V.24 is a serial interface with unbalanced data and control lines. A brief overview of RS232D/V.24 is given in Section 8. A comparison between several of the serial interfaces is provided in Section 7. Further references to RS232D should be assumed to include CCITT V.24. RS449 is a combination of balanced and unbalanced signals whose functions are analogs of the RS232D signals. A brief summary of this interface is given in Section 9.

4.2 Analysis Probe Function

The primary function of the ALD-232A is to convert the serial data stream into parallel data and status. It monitors five handshake lines and stores their states for each received character. In addition to converting the serial data to parallel data for the state display, the ALD-232A also provides the buffered serial signals directly to a second pod (pod 3) of the logic analyzer for a simultaneous timing display. The input buffers provide one RS232D standard load to the bus. Signals are inverted by the buffer circuitry.

4.3 Connection to the RS232/449 Bus

The ALD-232A provides a cable for connecting to the RS232D bus. This cable has 3 connectors, a male DB25 on one end, a female DB25 on the other and a 2x13 IDC connector in the center. The center connector should be plugged into the 2x13 male connector labeled J2 on the top of the ALD-232A. When RS232 is selected, the LED next to J2 will be illuminated. The other ends of the cable should be connected in line with the RS232 bus. The male and female connectors allow the ALD-232A to be inserted anywhere in the bus without the need for adapters or gender changers.

Some RS232D busses utilize connectors other than standard 25 pin DB25 connectors. The IBM PC frequently uses a 9 pin connector D connector. An adapter cable must be used in these instances to attach the ALD-232A. It is also possible to make a special cable with flat ribbon cable and a 2x13 IDC connector to attach to an arbitrary pinout.

Connection to the RS449 bus is similar. Use the cable provided with DB37 connectors on the ends and a 2x20 IDC connector in the center. The middle IDC connector should attach to the ALD-232A connector on the top panel labeled J3. When RS449 is selected, the LED next to J3 will be illuminated.

Since there are other synchronous, balanced serial bus connectors that utilize RS422 signaling standards, a custom cable may be used with the J3 connector. If you would like to create a custom cable for the ALD-232A, the table below shows the pinout of the appropriate pins on the 40 pin IDC connector.

+ sig	-sig	40 Pin IDC connector (RS449)	RS232 Equivalent Name
7	6	SD -Send Data	TXD
9	8	ST -Send Timing	DCE_SC
11	10	RD -Receive Data	RXD
13	12	RS -Request to Send	RTS
15	14	RT -Receive Timing	REC_SC
17	16	CS -Clear to Send	CTS
21	20	DM -Data Mode	DSR
23	22	TR -Terminal Ready	DTR
25	24	RR -Receiver Ready	CD
33	32	TT -Terminal Timing	DTE_SC
37		SG -Signal Ground	

The receive data signal pair (RD) is always clocked by the RT (Receive Timing) signal pair. The send data (SD) can be clocked either by ST or TT. The SYNC setup option in the ALD-232A allows the selection of either of these as the clock source. If you want ST for the SD clock, select “DCE Source” or if you want TT for the SD clock, select “DTE source”.

The logic analyzer cables from Pod 1 and Pod 3 should be connected to the right side of the ALD-232A to the indicated connectors, Pod 1 near the bottom and Pod 3 above it. *It is necessary to attach both cables even though only STATE analysis is desired.* This is because the ALD-232A derives its power from the logic analyzer and both cables are necessary to source adequate current.

RS232/RS449 Mode		
CHANNEL	POD1	POD3
CLK	Character valid strobe	REC SC
0	Character bit 0	CTS
1	Character bit 1	DTR
2	Character bit 2	TXD
3	Character bit 3	DSR
4	Character bit 4	RXD
5	Character bit 5	RTS
6	Character bit 6	CD
7	Character bit 7	REC SC
8	CTS	DTE SC
9	DTR	DCE SC
10	DSR	
11	RTS	
12	CD	
13	DISP MODE [0]	
14	DISP MODE [1]	
15	DIR	

Figure 2: ALD232A Pod Connections

Bits 15:8 on Pod 1 are used by the logic analyzer software to display the state of the RS232 status lines at the time the character was received. DISP MODE indicates to the logic analyzer software the display type to use:

- DISP MODE: 0 - ASCII
- 1 - EBCDIC
- 2 - TRANSCODE
- 3 - Special Character Received: The character field contains special formatting data (see below)

The DIR bit identifies from which channel, TX [=0] or RX [=1] that the data was received.

If DISP MODE=3 is received, the Character data field contains a code that indicates the type of error. This data has been sent by the ALD-232A and was NOT received from the RS232/449 bus. Each bit of the character code has a specific meaning associated with it:

Char. Bit	Meaning if DISP MODE = 3	
	SYNC	ASYNC
7	Normal End of Frame	-
6	CRC error	Framing error
5	RX Overrun	RX Overrun
4	Parity error	Parity error
3	ABORT	BREAK
2	not used	not used
1	not used	not used
0	=1 SYNC Flag	=0 ASYNC Flag

Pod 3 contains 3 serial clocks that are used in synchronous mode:

- REC SC Receive Synchronous clock
- DTE SC Transmit Synchronous clock, using the DTE as a source
- DCE SC Transmit Synchronous clock, using the DCE as a source

4.3.1 ALD-232A Setup

There are several parameters that affect the manner in which data is transferred over RS232D busses. These parametric choices must be entered into the ALD-232A in order for it to properly interpret the data. The keyboard and display on the ALD-232A are used to enter these data.

The cable to the bus under test is connected to the ALD-232A at the connector which has the LED illuminated.

For RS232 async operation, the screen below will be shown:

```
<-  RS232 ASYNC  ->
TX: 4E
RX: 20    DSR
Baud rate 9600
Bits/char 8
Stopbits 2
Parity NO
Type ASCII
```

These are the most recent values seen on the bus (HEX)

The active control lines are shown in this area

These values are set by the user

For RS232 sync operation, the screen below will be shown:

```
<-  RS232 ASYNC  ->
TX: 4E
RX: 20    DSR
TX CLK from DCE
CRC Seed FFFF
```

DCE or DTE

0000 or FFFF

These options are set by using the ▼ and ▲ to get to the correct line in the display and then using ◀ or ▶ to select the correct choice.

The choices for RS449 operation are the same.

4.3.2 Logic Analyzer Setup

After the ALD-232A has been set up, the logic analyzer must be configured. The configuration file appropriate to the logic analyzer card must be selected by the logic analyzer's file manager. (See Installation section 1.3.)

This will load both the data formatter (a.k.a. inverse assembler) and the configuration. The data formatter provides a multi-column display of the capture data, indicating which channel (TX or RX) received the character and columns for each control line.

The workspace for the RS232 configuration is shown in Figure 3 below:

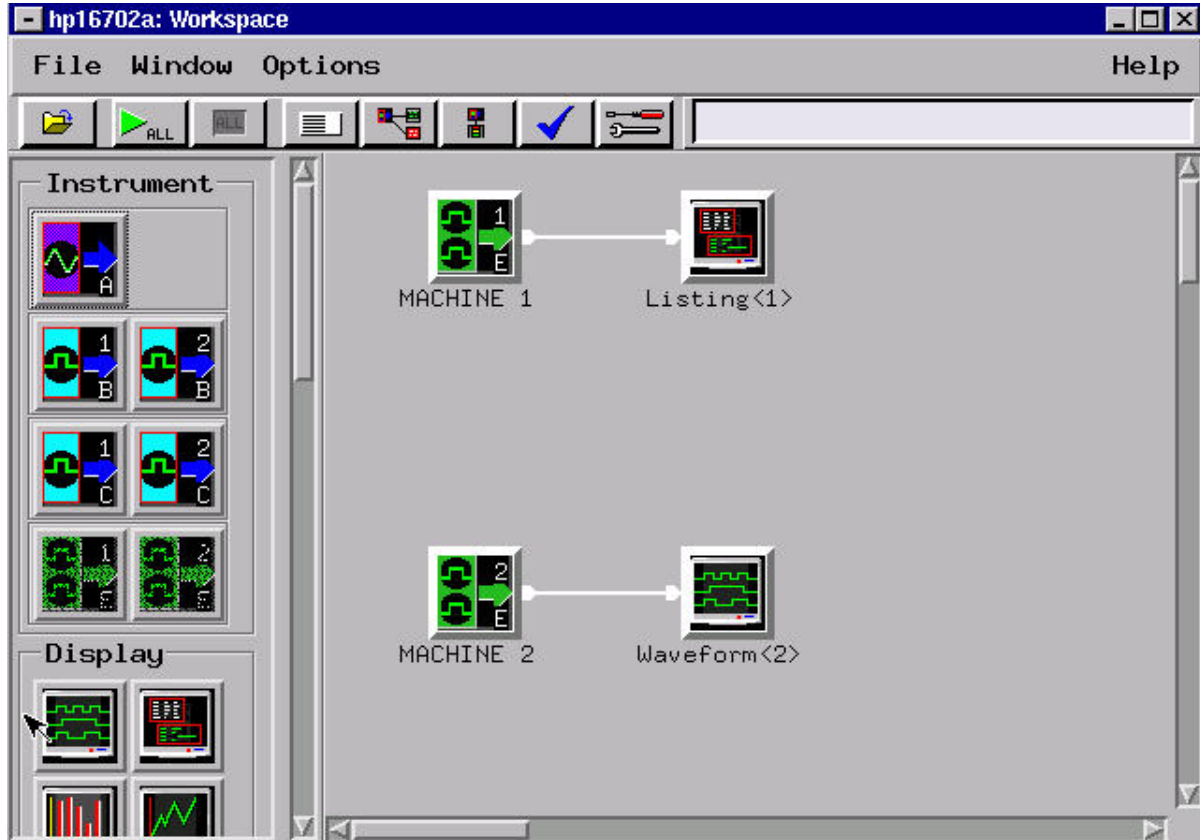


Figure 3: RS232 Workspace

MACHINE 1 is configured for POD1 (State Analysis) and MACHINE 2 is configured for POD3, timing analysis. The formats for these machines are shown in Figure 4 and Figure 5 on the next page.

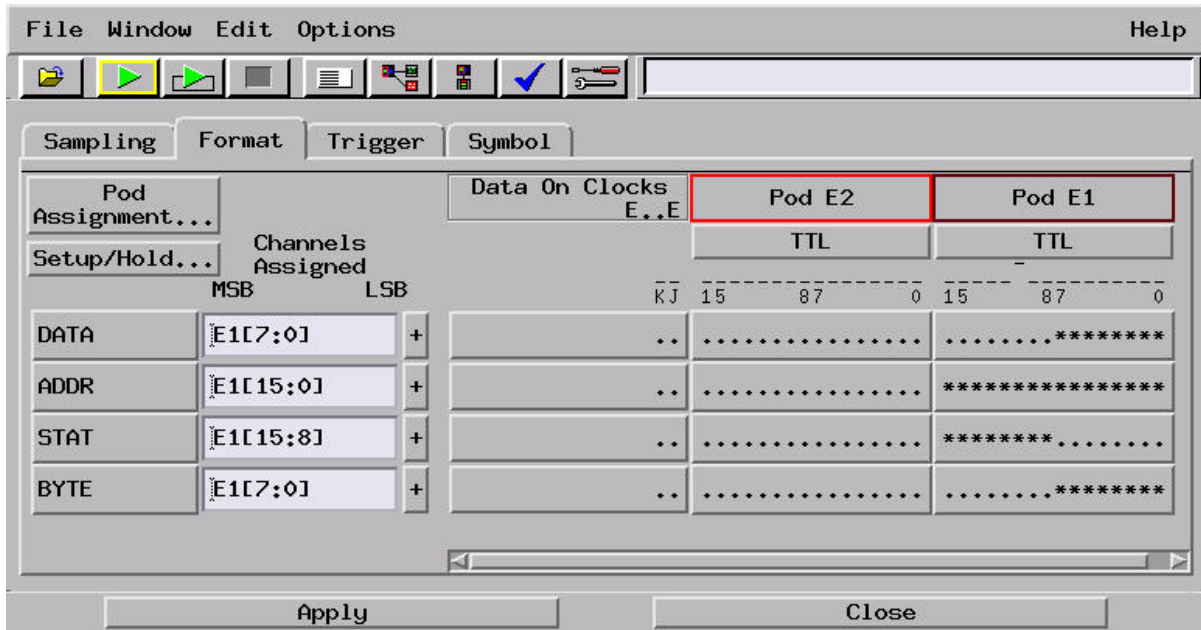


Figure 4: RS232 State Format

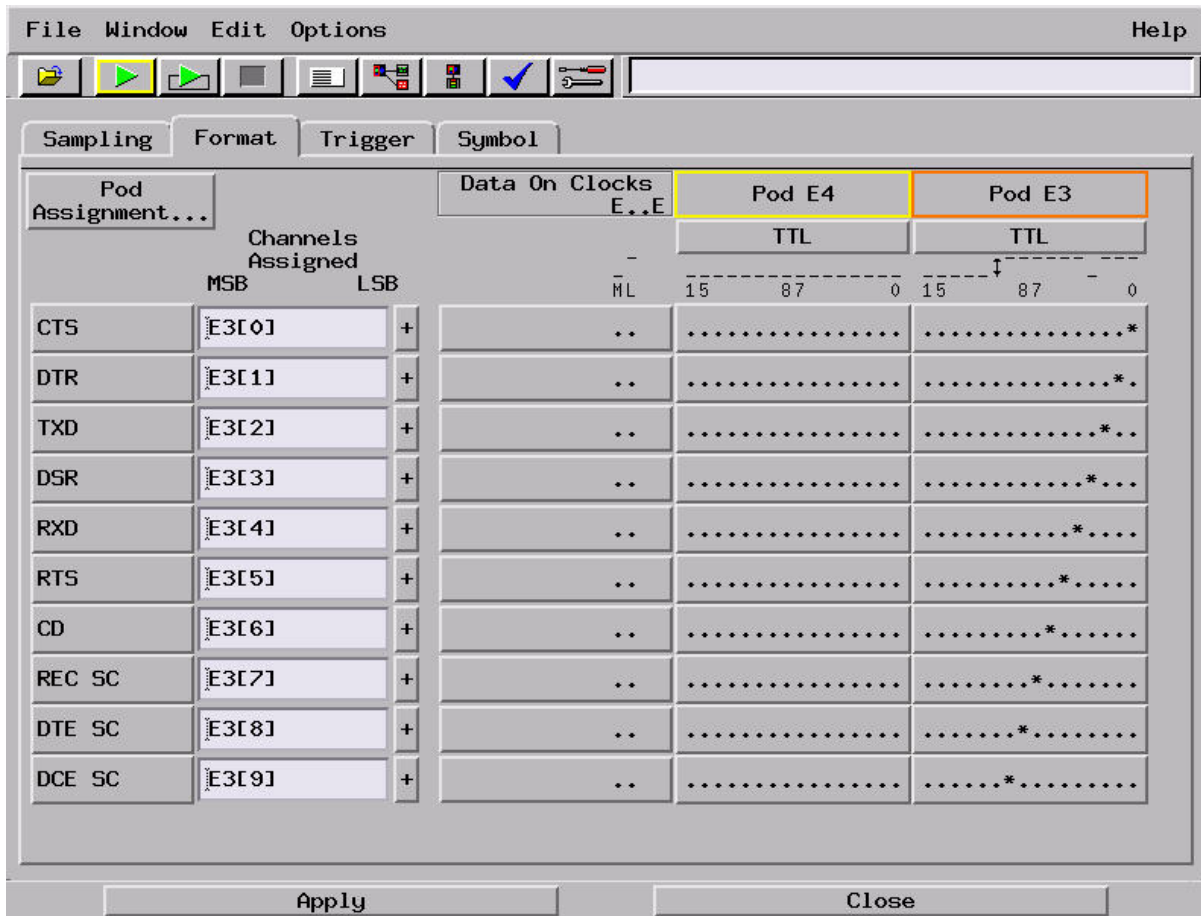


Figure 5: RS232 Timing Format

In the ASYNC state display, the important field is the **RS232/RS449 Data Formatter** field. The **ADDR**, **DATA** and **STAT** fields are of no particular interest and are included as a consequence of the logic analyzer operation. They may be deleted by the user if desired.

The 167xx logic analyzer provides for filtering and coloring of the displayed data. Select **INVASM**, then **FILTER** from the LISTING window.

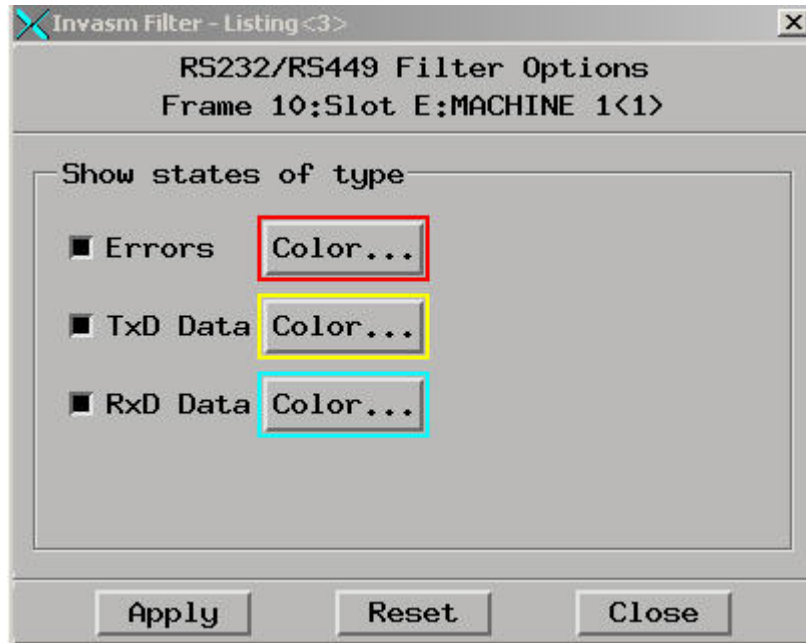


Figure 6: Serial Filter Options

Using this menu, the operator may choose the color for TXD and RXD as well as the color for any error displays. In addition, TXD, RXD or Errors may be suppressed from the display by unchecking the box to the left.

The timing machine is completely separate from the state capture. They may be linked or used to capture a different time section of the input serial stream. To see the timing associated with the State display, select "Wait for second analyzer to trigger" in the timing trigger setup menu. Another useful option is to select "Transitional" recording under the **Sampling** tab of the timing setup window. This provides more data length for the timing display.

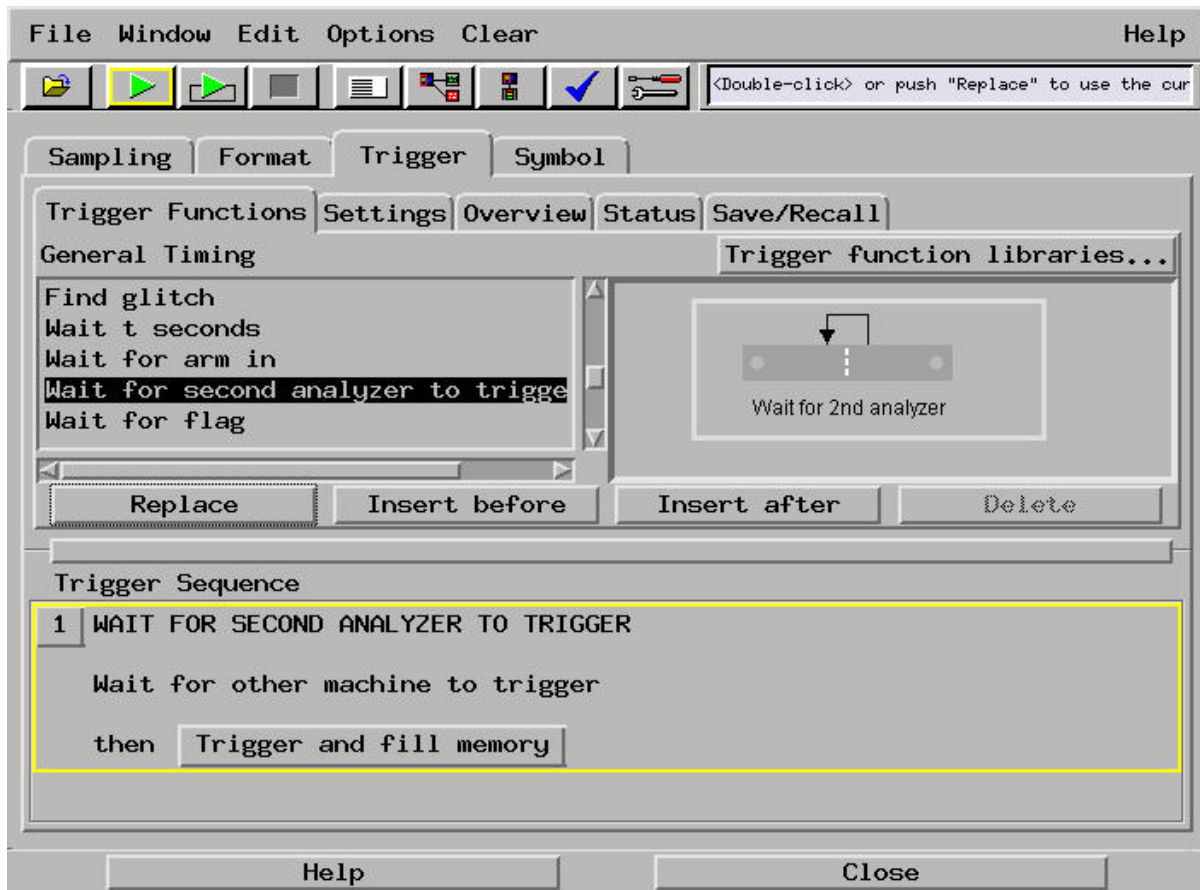


Figure 7: Timing Setup for correlated State/Timing

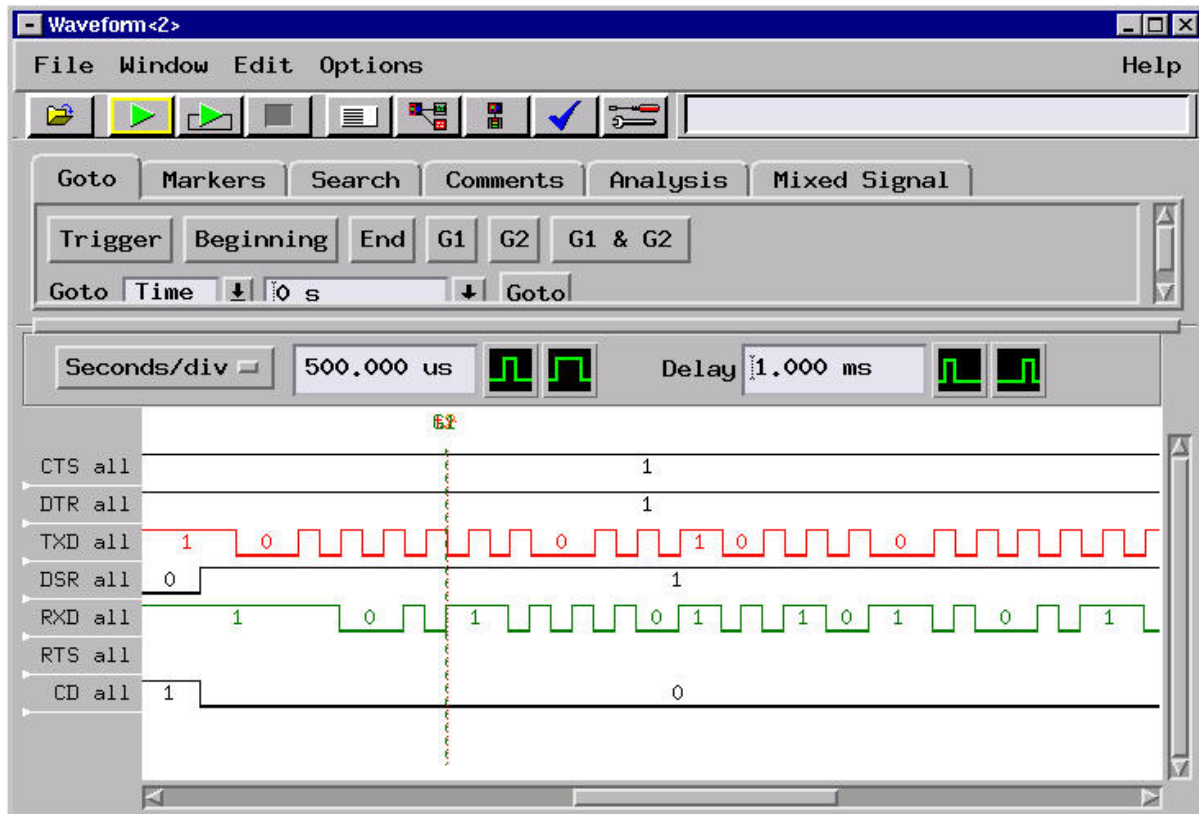


Figure 8: Example of Async Timing Display

4.4 Synchronous Data Display

The data formatter supplied with the ALD-232A interprets data for the state display in synchronous mode as well as asynchronous mode.. An example of a state display of synchronous data is shown in Figure 9:

Listing<1>

File Window Edit Options Invasm Source Help

Goto Markers Search Comments Analysis Mixed Signal

Trigger Beginning End G1 G2

Goto Time ↓ 0 s ↓ Goto

State Number	ADDR	RS232/RS449 Data Formatter							DATA	STAT	BYTE	Time
		TxD	RxD	RTS	CTS	DTR	DSR	CD				
0	6009	ERROR		ABORT				09	60	09		
1	E009			ERROR		ABORT		09	E0	09	124,000 ns	
2	0054	T						54	00	54	1,771 ms	
3	8074		t					74	80	74	104,216 us	
4	0045	E						45	00	45	729,144 us	
5	8065		e					65	80	65	104,188 us	
6	0053	S						53	00	53	729,144 us	
7	8073		s					73	80	73	104,184 us	
8	0054	T						54	00	54	729,180 us	
9	8074		t					74	80	74	104,184 us	
10	0045	E						45	00	45	729,144 us	
11	8065		e					65	80	65	104,184 us	
12	0052	R						52	00	52	729,148 us	
13	8072		r					72	80	72	104,216 us	
14	0054	CRC						54	00	54	729,144 us	
15	80FC		CRC					FC	80	FC	208,372 us	
16	0011	CRC						11	00	11	624,960 us	
17	807A		CRC					7A	80	7A	208,372 us	
18	6081	EOF						81	60	81	624,992 us	
19	E081		EOF					81	E0	81	208,340 us	
20	0054	T						54	00	54	8,125 ms	
21	8074		t					74	80	74	208,372 us	
22	0045	E						45	00	45	624,992 us	
23	8065		e					65	80	65	208,340 us	
24	0053	S						53	00	53	624,992 us	
25	8073		s					73	80	73	208,372 us	
26	0054	T						54	00	54	624,956 us	
27	80B7		CRC					B7	80	B7	208,372 us	
28	0045	E						45	00	45	624,992 us	
29	8046		CRC					46	80	46	208,340 us	
30	0052	R						52	00	52	624,988 us	
31	E081		EOF					81	E0	81	208,372 us	
32	0054	CRC						54	00	54	624,992 us	
33	8074		t					74	80	74	208,340 us	
34	0011	CRC						11	00	11	624,988 us	
35	8065		CRC					65	80	65	208,372 us	

Figure 9: RS232D Synchronous State Display

4.5 Asynchronous Data Display

The data formatter will present data in the same way for asynchronous data as it does for synchronous data. It differs in that data is not framed and no CRCs are present. The data formatter does check for the usual asynchronous errors: framing, parity, overrun and break.

The state analysis is viewed by displaying Listing(1) from the workspace and the timing is viewed by displaying Waveform(2) from the workspace.

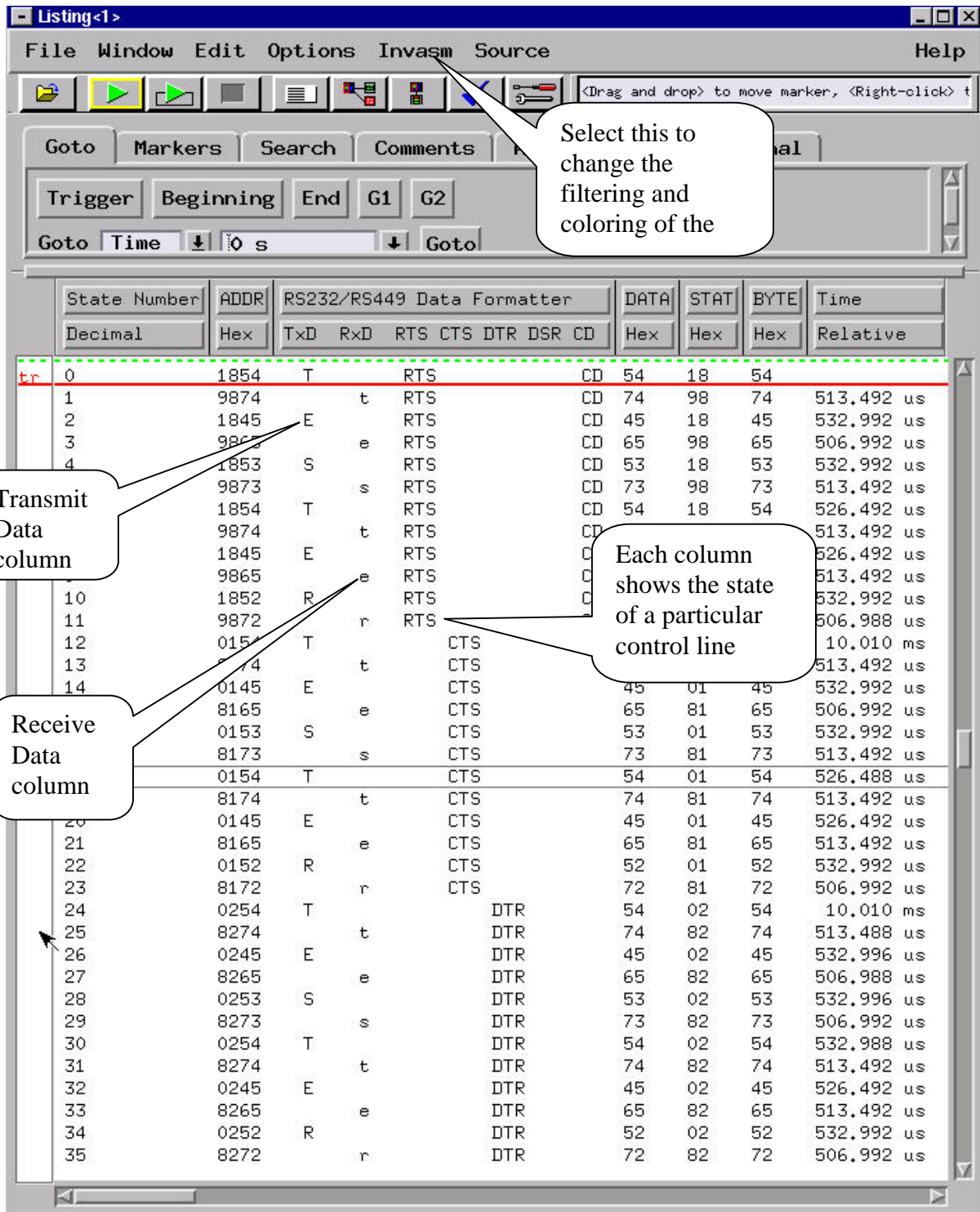


Figure 10: Asynchronous State Display

This example shows the presentation of active control lines [RTS, CTS, DTR, and DSR] and interleaved asynchronous data. When the data represents a special character in the requested

data set [ASCII, Transcode or EBCDIC], that character is displayed between “<>”. The data is always presented in hex format under the *BYTE* label.

5. Analyzing IEEE1284

5.1 Introduction

The popular Centronics® parallel printer port has been enhanced to support bi-directional communications. The IEEE has released a specification for communication based upon work done by Hewlett-Packard in the Boise Division, the IEEE1284. This specification identifies several methods of communication: compatibility mode (formerly known as Centronics mode), nibble mode, byte mode, ECP and EPP modes. At present, the ALD-232A supports compatibility, nibble and ECP modes.

5.2 Analysis Probe Function

The ALD-232A analysis probe captures data in both directions from the IEEE1284 bus and presents that data to the logic analyzer. The analysis probe has a state-tracking machine that follows the parallel bus control lines and determines which mode, compatibility, nibble or ECP in which the bus is operating. When data is detected, the ALD-232A will present that data, either as a byte in all but the nibble mode, or a nibble in nibble mode, to the logic analyzer. The software in the logic analyzer will collect the reverse channel nibbles in nibble mode and the bytes in all other modes, and display that data in one of 2 columns depending upon the direction. One column, MODE, indicates which mode has been detected (nibble, compatibility or ECP).

5.3 Connection to the IEEE1284 Bus

A Y-cable is provided with the ALD-232A that has a male DB25 on one end, a female DB25 on the other end and a 2x13 female IDC connector in the center. Insert this cable into the IEEE1284 bus by using the DB25 connectors. The center connector is attached to the connector on the top panel of the ALD-232A using the 2x13 IDC connector at the connector marked J1 (the adjacent LED will be lit when IEEE1284 is selected).

5.4 Connection to the Logic Analyzer

The logic analyzer cables from Pod 1 and Pod 3 should be connected to the right side of the ALD-232A to the indicated connectors, Pod 1 near the bottom and Pod 3 above it. *It is necessary to attach both cables* even though only STATE analysis is desired. This is

because the ALD-232A derives its power from the logic analyzer and both cables are necessary to source adequate current.

IEEE1284		
CHANNEL	POD1	POD3
CLK	Data Strobe	nSTB
0	Data 0	D0
1	Data 1	D1
2	Data 2	D2
3	Data 3	D3
4	Data 4	D4
5	Data 5	D5
6	Data 6	D6
7	Data 7	D7
8	nFAULT (Nibble 0)	nSTB
9	SELECT (Nibble 1)	nFAULT
10	PERR (Nibble 2)	SELECT
11	BUSY (Nibble 3)	PERR
12	DispCode 0	BUSY
13	DispCode 1	nAUTOFD
14	DispCode 2	nACK
15	nINIT	nSELIN

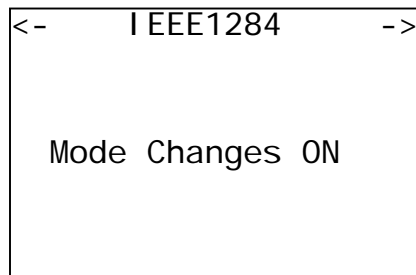
Table 1: IEEE1284 Pod Connections

Bits 14:12 on Pod 1 are used by the logic analyzer software to identify the type of data being sent to the logic analyzer:

DispCode	Data Type
7	Compatibility Data
0	Rev. Nibble Low
1	Rev. Nibble High
2	Fwd. ECP
3	Rev. ECP

5.5 ALD-232A Setup

To select IEEE1284 analysis, simply move the cursor (->) to the top of the screen on the ALD232A (if it is not already there) and use the ◀ or ▶ keys until the following screen appears:



This is all that is necessary to place the ALD232A into IEEE1284 mode. The only choice the user may select is whether (or not) to select the display of mode or phase changes as the IEEE1284 interface progresses. The modes are:

- Compatibility Mode
- Nibble Mode
- ECP Mode
- Request ID (Nibble)
- Request ID (ECP)

To enable the display of these mode changes when they occur, use the ▼ key to move the cursor to the Mode Change option and then use the ◀ or ▶ keys to toggle that option between ON and OFF.

5.6 Logic Analyzer Setup

From the */logic/configs/ALD/ALD-232-IE1284* directory, load the configuration appropriate to the logic analyzer card installed in your 167xx analyzer. This will automatically load the data formatter software into the logic analyzer.

The workspace loaded is shown in Figure 11 on the next page. Both State and Timing are captured separately and may be displayed simultaneously. Since both machines have their own trigger conditions, the user is free to configure these as related or unrelated. It is commonly done that the State machine is used to capture the item(s) of interest and the Timing machine will examine the waveforms in that area. To accomplish this, the Timing trigger must be configured as "Wait for second analyzer to trigger" and probably the sampling should be set to "Transitional" recording to preserve as much trace depth as possible. (See Figure 7: Timing Setup for correlated State/Timing.)

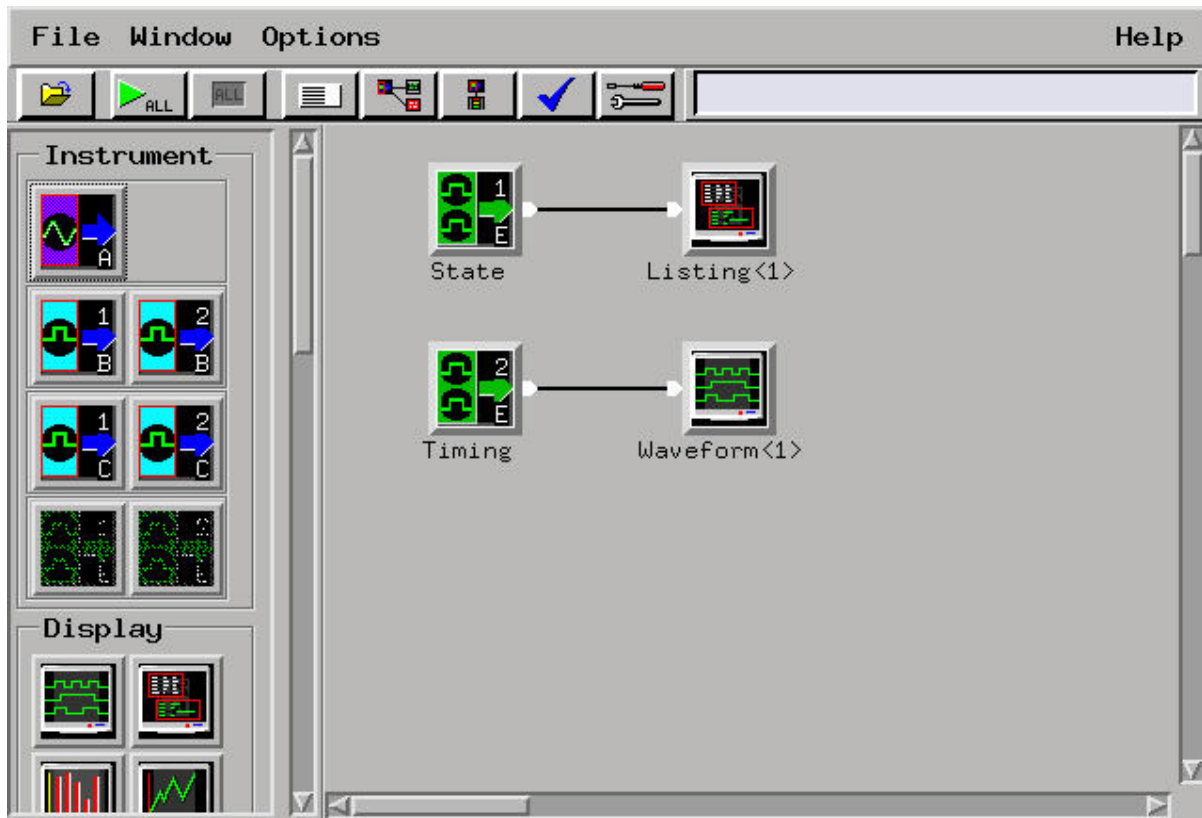


Figure 11: IEEE1284 Workspace

5.7 IEEE1284 Display

State Number	ADDR	1284 Format	DATA	STAT	Time
Decimal	Hex	MODE FWD REV	Hex	Hex	Relative
295	8404		04	04	96.532 us
296	8630	NIB 0	30	06	58.216 us
297	8404		04	04	95.372 us
298	8643	NIB C	43	06	57.404 us
299	8404		04	04	99.844 us
300	863B	NIB ;	3B	06	57.344 us
301	B004	>>> COMP MODE	04	30	44.124 us
302	FF00	<NUL>	00	7F	6.510 s
303	FF00	<NUL>	00	7F	7.844 us
304	FF00	<NUL>	00	7F	8.376 us
305	FF0A	<LF >	0A	7F	7.184 us
306	FF41	A	41	7F	7.312 us
307	FF42	B	42	7F	7.312 us
308	FF43	C	43	7F	8.504 us
309	FF44	D	44	7F	7.344 us
310	FF45	E	45	7F	8.496 us
311	FF46	F	46	7F	7.316 us
312	8710	>>> ECP MODE	10	07	2.030 s
313	B010	>>> COMP MODE	10	30	1.971 s
314	8E14	>>> REQ ID ECP	14	0E	773.236 us
315	0C00	ECP <NUL>	00	0C	247.528 us
316	0C00	ECP <NUL>	00	0C	11.028 us
317	0C96	ECP 96h	96	0C	41.160 us
318	0C56	ECP V	56	0C	41.188 us
319	0C53	ECP S	53	0C	41.216 us
320	0C54	ECP T	54	0C	41.248 us
321	0C41	ECP A	41	0C	41.216 us
322	0C54	ECP T	54	0C	41.220 us
323	0C55	ECP U	55	0C	41.188 us
324	0C53	ECP S	53	0C	41.184 us
325	0C3A	ECP :	3A	0C	41.220 us
326	0C24	ECP *	24	0C	41.156 us
327	0C48	ECP H	48	0C	41.188 us
328	0C30	ECP 0	30	0C	41.216 us

Figure 12: IEEE1284 State Display

In this example, the IEEE1284 bus starts in nibble mode, transitions to compatibility mode and finally ends in ECP mode. Each mode change is indicated with a line prefaced with ">>>". The FWD data column displays data in the normal direction (computer to printer) and the REV data column shows data from the printer back to the computer.

As with the RS232 display, the user can selectively color and display different types of data. Click the **INVASM** item in the menu bar. It will invoke the following selector box:

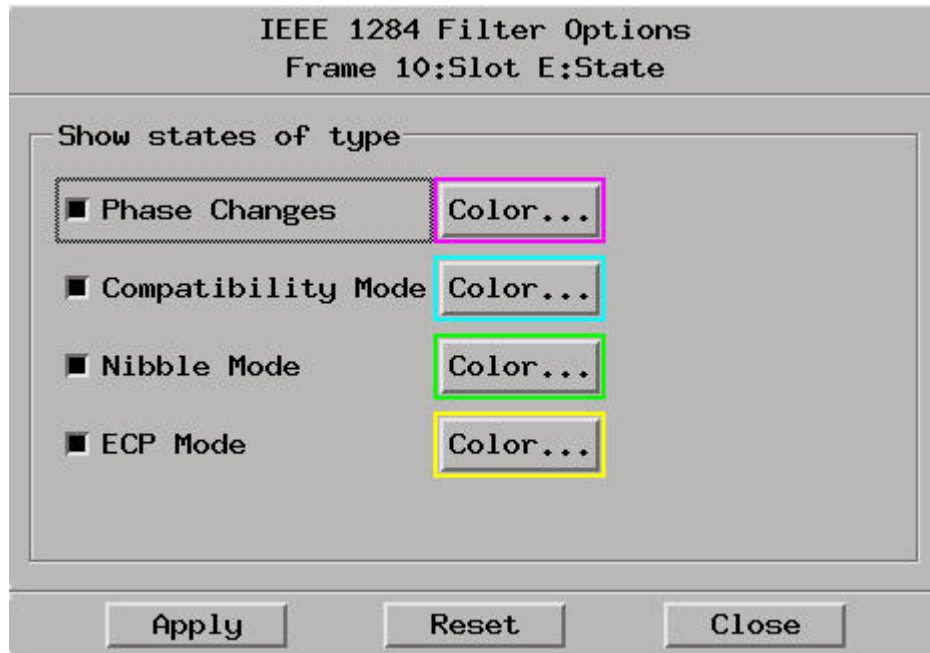


Figure 13: IEEE1284 State Color and Filter Dialog

In this dialog box, the user may choose to display/not display data in a particular mode or the phase changes between modes and may also choose a particular color for that event.

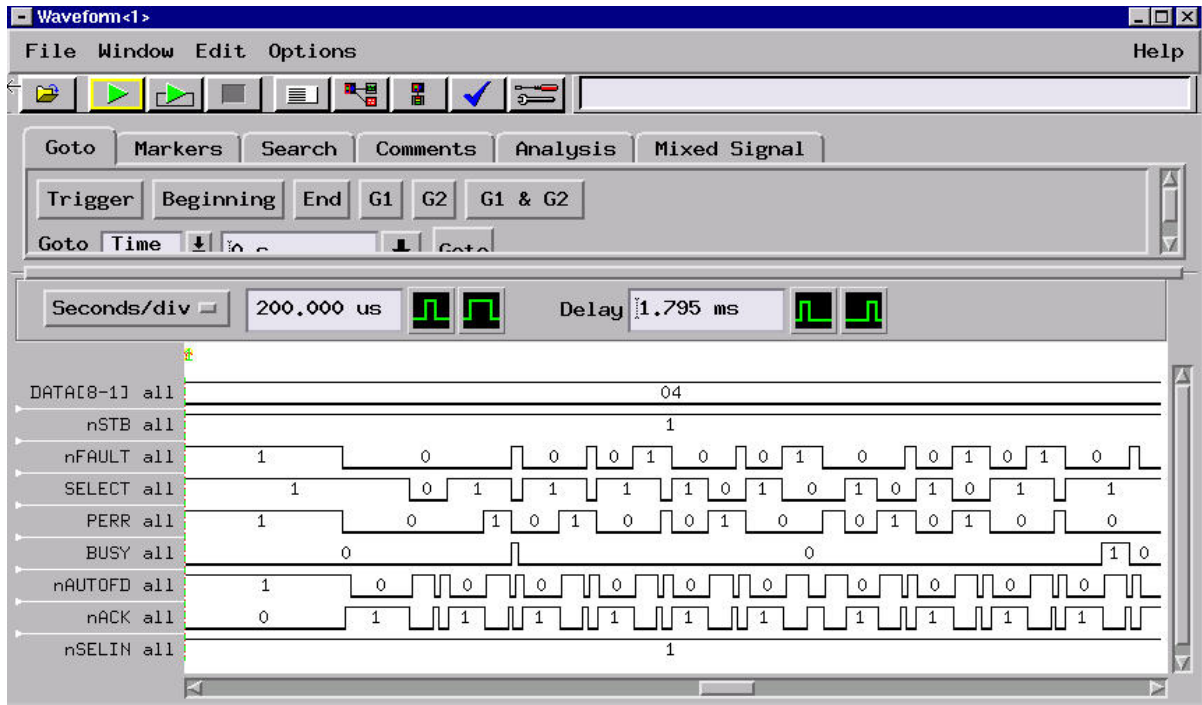


Figure 14: IEEE1284 Timing Display

6. Theory of Operation

The block diagram of the ALD-232A analysis probe is shown below:

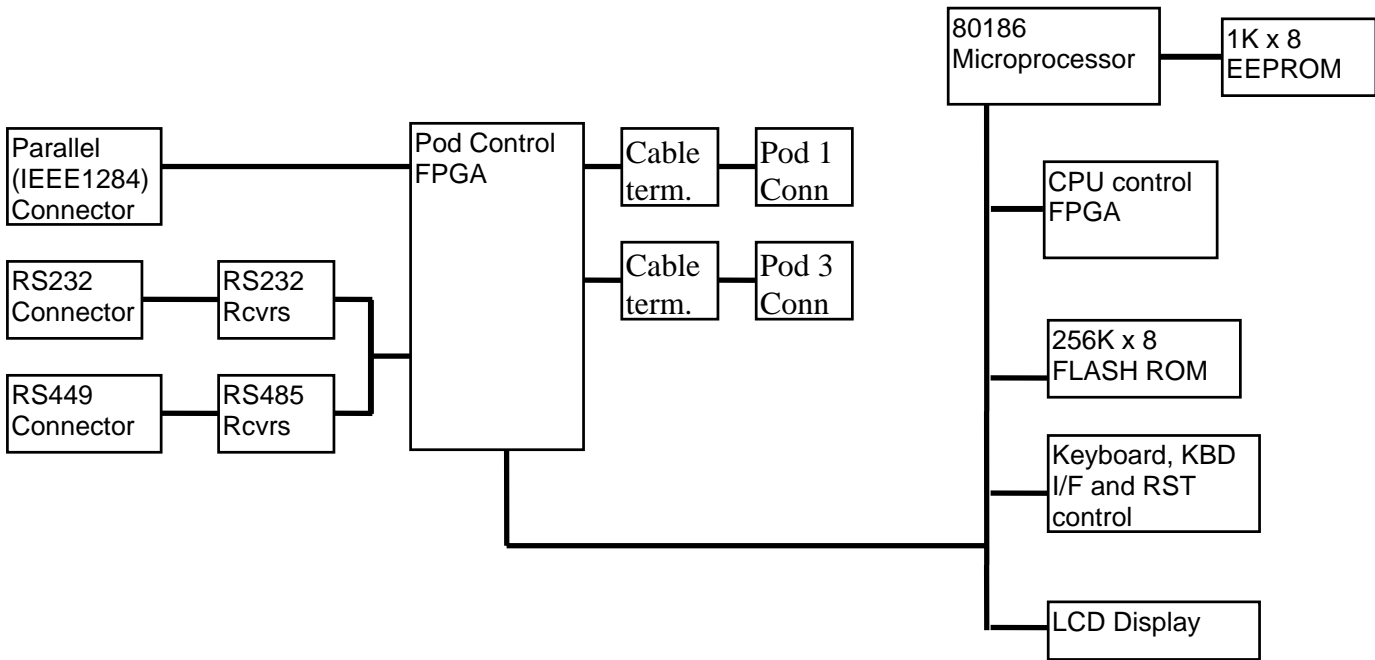


Figure 15: ALD232A Block Diagram

The ALD-232A is a complete small processor system, with RAM, ROM, keyboard and display and a data capture system. The microprocessor system downloads the FPGAs with code appropriate to the operation selected, and receives parametric data from the user to program both FPGAs .

The 80186ER microprocessor system is conventional in design with the processor running at 32 MHz. Each time that the user selects a new parameter or option and hits the ENTER key, that selection is recorded in the EEPROM. Data is also stored in the EEPROM after any mode change persists for more than 5 secs. This allows that selection to survive power loss. The Flash PROM contains not only the operational code, but also binary images of the code in both FPGAs. The CPU Control FPGA is downloaded automatically from the FPRM prior to the release of RESET from the 186. The Pod Control FPGA is downloaded under program control with code for RS232, RS449 or IEEE1288 or any option than may be included,

The Pod Control FPGA collects data from the appropriate interface, RS232, RS449, or IEEE1284 and presents it to the pins of the logic analyzer. The FPGA acts as a dual UART or USRT.

In the case of RS232 or RS449 data, the Pod Control FPGA selects the appropriate data receiver. Both sets of receivers are connected to the same internal signals and the inoperative set of receivers is tri-stated. These signals feed the FPGA. The FPGA itself contains a dual USART for converting the serial bit stream into parallel characters and special flag characters for the logic analyzer's data formatter to interpret.

When IEEE1284 is selected, a state-tracking machine is loaded in Pod Control. This machine tracks the state of the control and data lines of the parallel interface and when a character has been detected, it sends that data to the logic analyzer. It also sends a code identifying the data as forward compatibility data or reverse nibble data and which nibble it is.

7. Serial Interface Comparisons

Following are several tables that show comparisons between serial interfaces covered in this document as well as interfaces not directly covered. Those not directly covered in this document are shown here for reference purposes.

INTERFACE NAME	MECHANICAL STANDARD	ELECTRICAL STANDARD	FUNCTIONAL STANDARD
RS232D	RS232D	RS232D	RS232D
CCITT V.24	ISO-2110	CCITT V.28	CCITT V.24
MIL-188C	RS232D	MIL-188C	RS232D
RS449 (balanced)	RS449	RS422	RS449
RS449 (unbalanced)	RS449	RS423	RS449
CCITT V.35 (balanced)	ISO-2593	CCITT V.11 (X.27)	CCITT V.24
CCITT V.35 (unbalanced)	ISO-2593	CCITT V.10 (X.26)	CCITT V.24
MIL-188-114 (balanced)	MIL-188-114	MIL-188-114	MIL-188-114
CCITT X.20 (no clocks)			
CCITT X.21 (clocks)	ISO-4903	CCITT V.11	CCITT X.27
CCITT X.21 -bis	RS232D	CCITT V.10	CCITT X.26

Table 2: Serial Interface Standards Comparison

INTERFACE TYPE	CONNECTOR	SPEED	ELECTRICAL MAXIMUM	THRESHOLD
RS232D	25 pin	<115.2Kbps	±25V	±3V
RS449 RS422 (balanced) RS423 (unbalanced)	37 pin	<10Mbps <100Kbps	±6V	±0.2V
CCITT V.35	34 pin	56Kbps	(bipolar	current)
CCITT X.20/X.21	15 pin		±10V	±0.3V
CCITT V.10 (unbalanced) CCITT V.11 (balanced)		<100Kbps <10Mbps		

Table 3: Serial Interface Characteristics Comparison

DTE / DCE	EIA RS232D		CCITT V.24		EIA RS449		
→ ←	AB	Signal Ground	102	Signal Ground	SG	Signal Ground	
			102a	DTE Common	SC	Send Common	
			102b	DCE Common	RC	Receive Common	
→ ← → ←	CE	Ring Indicator	125	Calling Indicator	IS	Terminal In Service	
	CD	Data Terminal Ready	108.2	Data Terminal Ready	IC	Incoming Call	
	CC	Data Set Ready	107	Data Set Ready	TR	Terminal Ready	
					DM	Data Mode	
→ ←	BA	Transmitted Data	103	Transmitted Data	SD	Send Data	
	BB	Received Data	104	Received Data	RD	Receive Data	
→ ← ←	DA	Transmitter Signal Element Timing (DTE Source)	113	Transmitter Signal Element Timing (DTE Source)	TT	Terminal Timing	
	DB	Transmitter Signal Element Timing (DCE Source)	114	Transmitter Signal Element Timing (DCE Source)	ST	Send Timing	
	DD	Receiver Signal Element Timing	115	Receiver Signal Element Timing (DCE Source)	RT	Receive Timing	
→ ← ← ← → → → ←	CA	Request to Send	105	Request to Send	RS	Request to Send	
	CB	Clear to Send	106	Ready for Sending	CS	Clear to Send	
	CF	Received Line Signal Detector	109	Data Channel Received Line Signal Detector	RR	Receiver Ready	
	CG	Signal Quality Detector	110	Data Signal Quality Detector	SQ	Signal Quality	
					NS	New Signal	
				126	Select Transmit Frequency	SF	Select Frequency
	CH	Data Signal Rate Selector (DTE Source)	111	Data Signaling Rate Selector (DTE Source)	SR	Signaling Rate Selector	
	CI	Data Signal Rate Selector (DCE Source)	112	Data Signaling Rate Selector (DCE Source)	SI	Signaling Rate Indicator	
→ ←	SBA	Secondary Transmitted Data	118	Transmitted Backward Channel Data	SSD	Secondary Send Data	
	SBB	Secondary Received Data	119	Received Backward Channel Data	SRD	Secondary Receive Data	
→ ← ←	SCA	Secondary Request to Send	120	Transmit Backward Channel Line Signal	SRS	Secondary Request to Send	
	SCB	Secondary Clear to Send	121	Backward Channel Ready	SCS	Secondary Clear to Send	
	SCF	Secondary Received Line Signal Detector	122	Backward Channel Received Line Signal Detector	SRR	Secondary Receiver Ready	
→ → ←			141	Local Loopback	LL	Local Loopback	
			140	Remote Loopback	RL	Remote Loopback	
			142	Test Indicator	TM	Test Mode	
→ ←			116	Select Standby	SS	Select Standby	
			117	Standby Indicator	SB	Standby Indicator	

Table 4: Serial Interface Interchange Circuit Comparison

8. RS232C/CCITT V.24 Overview

8.1 Introduction

The RS232D/CCITT V-24 is a serial interface standard that has predominated for many years. It originated with the requirements for teletype interface, which accounts for the large voltage specifications in the standard. It is still being designed into new equipment though it

is being replaced by the RS449 standard, due to the much higher data speeds of RS449. The RS232D is the EIA standard conforming to the international standard CCITT V.24. It expands on the international standard to include the connector type, pin assignments, and electrical standards.

The following information is intended to be a coverage of the main points of RS232D. A person needing comprehensive information about the standard should obtain the related documents from the EIA. Many books and other documents have been written that cover RS232D and its many idiosyncrasies and permutations.

8.2 The RS232D/CCITT V.24

Within the context of the above paragraphs, most voltage interfaces in North America conform to EIA RS232D. This specifies a 25-pin connector as the standard interface in datacom networks. The connector is shown in figure 16. The interchange circuitry with pin assignments and CCITT V.24 equivalents is shown in table 5. In addition to the mechanical and electrical requirements, it specifies an operating range of 0 to 20K bps in bit-serial operation, synchronous and asynchronous operation.

8.2.1 Mechanical

The interface between the Data Communications Equipment (DCE), usually a modem, and the Data Terminal Equipment (DTE), the remote terminal or data processor, is located at the RS232D specified connector located between two equipments. The female is connected to the DCE and the male to the DTE. Short cables of less than 15 meters (50 feet) are recommended, but longer cables may be used if the load capacitance is suitable. The pin assignments shown in figure 16 must be used; unassigned pins may carry additional circuits determined by mutual agreement between the communicating parties.

While RS232D designates 23 circuits, the number actually used in a given application depends on the requirements of the application. In the case of some modems only nine of the 23 are used.

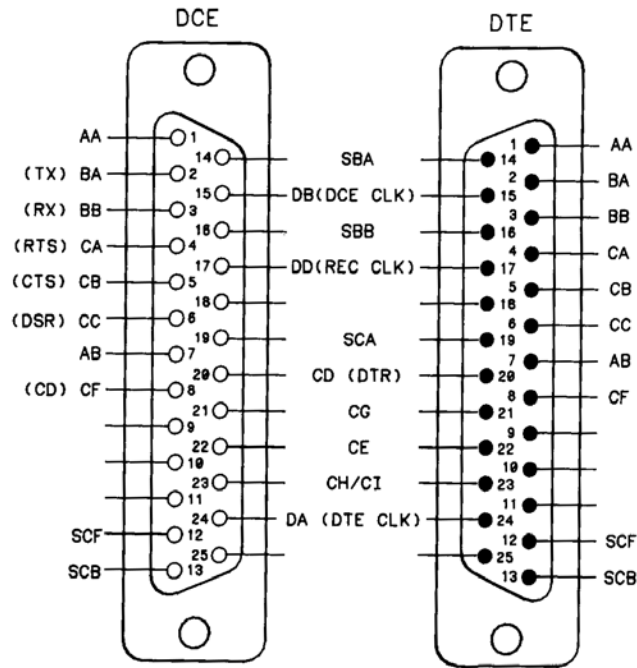


Figure 16: RS232 Connector with Assignments

8.2.2 Electrical

Except for protective and signal grounds, all circuits carry bi-polar low-voltage signals that are suitable for electronic circuits. All voltages are measured at the connector with respect to und (AB) and cannot exceed $\pm 25V$.

The electrical specifications are shown in table 3.

Control circuits can be designated as fail safe. This means that when power is lost at the transmitter the receiver interprets the signal condition as off.

PIN	DIRECTION		RS232D CIRCUIT	CCITT V.24 CIRCUIT	RS232D DESCRIPTION
	DTE	DCE			
1	-		AA	101	Protective Ground
2	→		BA	103	Transmitted Data
3	←		BB	104	Received Data
4	→		CA	105	Request to Send
5	←		CB	106	Clear to Send
6	←		CC	107	Data Set Ready
7			AB	102	Signal Ground (Common Return)
8	←		CF	109	Received Line Signal Detector
9	-		-	-	(Reserved for Data Set Testing)
10	-		-	-	(Reserved for Data Set Testing)
11	-		-	-	Unassigned
12	←		SCF	122	Secondary Received Line
	-		-	-	Signal Detector
13	←		SCB	121	Secondary Clear to Send
14	→		SBA	118	Secondary Transmitted Data
15	←		DB	114	Transmitter Signal Element Timing
	-		-	-	(DCE Source)
16	←		SBB	119	Secondary Received Data
17	←		DD	115	Receiver Signal Element Timing
	-		-	-	(DCE Source)
18	-		-	-	Unassigned
19	→		SCA	120	Secondary Request to Send
20	→		CD	108.2	Data Terminal Ready
21	←		CG	110	Signal Quality Detector
22	←		CE	125	Ring Indicator
23	→		CH/CI	111/112	Data Signal Rate Selector
					(DTE/DCE Source)
24	→		DA	113	Transmitter Signal Element Timing
					(DTE Source)
25	-		-	-	Unassigned

Table 5: Interchange Circuits for RS232D and CCITT V.24 Equivalents

Driver output levels with 3KΩ to 7KΩ load	15V > V _{oh} > 5V -5V > V _{ol} > -15V
Driver output voltage with open circuit	V _o < 25V
Driver output impedance with power off	R _o > 300Ω
Output short circuit current	I _o < 0.5A
Driver slew rate	dv/dt < 30V/μS
Receiver input impedance	7KΩ > R _{in} > 3K
Receiver input voltage	±15V compatible with driver
Receiver output with open circuit input	MARK
Receiver output with +3V input	SPACE
Receiver output with -3V input	MARK
+15 >	LOGIC -0- = SPACE = CONTROL ON
+5 >	
+5 >	Noise Margin
+3 >	
+3 >	Transition Region
-3 >	
-3 >	Noise Margin
-5 >	
-5 >	LOGIC -1- = MARK = CONTROL OFF
-15 >	

Table 6: Condensed Electrical Specifications for EIA RS232D

9. RS449 and RS422 Overview

9.1 Introduction

In 1975 uniform standards were established governing the electrical parameters and interface between both high speed and low speed data communications. These standards, RS422 and RS423 respectively, specify those characteristics without defining the mechanical interface. RS422 establishes characteristics of balanced voltage interface circuits while RS423 establishes characteristics for unbalanced circuits.

The new standard for defining the mechanical and functional characteristics of the RS422 and RS423 standards is RS449. This standard was released in 1977. Only the RS422 standard will be presented further in this appendix.

9.2 The RS449/RS422

The main differences between the RS449 standard and the RS232D standard are the following:

1. Two connectors, a 37-pin and a 9-pin are used in place of the 25-pin connector used in RS232D applications. The 37-pin connector accommodates the normal interchange circuits while the 9-pin connector is used for secondary channel circuits. Both connectors are from the same family as the RS232D connector.
2. Depending on signaling rate, the cable distance between equipments has been extended to 60 meters (200 feet) from the RS232D distance of 15 meters (50 feet).
3. Ten interchange circuits not previously included in RS232D have been defined in RS449.
4. The electrical characteristics (RS422 and RS423) in the interface have been completely re-defined. Both balanced and unbalanced type circuits may be used within one interface connection. Two categories of circuits are defined: Category I circuits, which may be balanced or unbalanced depending on data rate, and Category II circuits which are always unbalanced.

With a few additional provisions, equipment conforming to this new standard can interoperate with equipment designed to RS232D.

9.3 Mechanical and Functional

The basic functional characteristic of the new standard (RS449) is operation up to a nominal limit of 2Mbps in synchronous or non-synchronous communication. The connector is shown in figure 17 on the next page. Table 7 shows the interchange circuits with pins, circuit names and mnemonics.

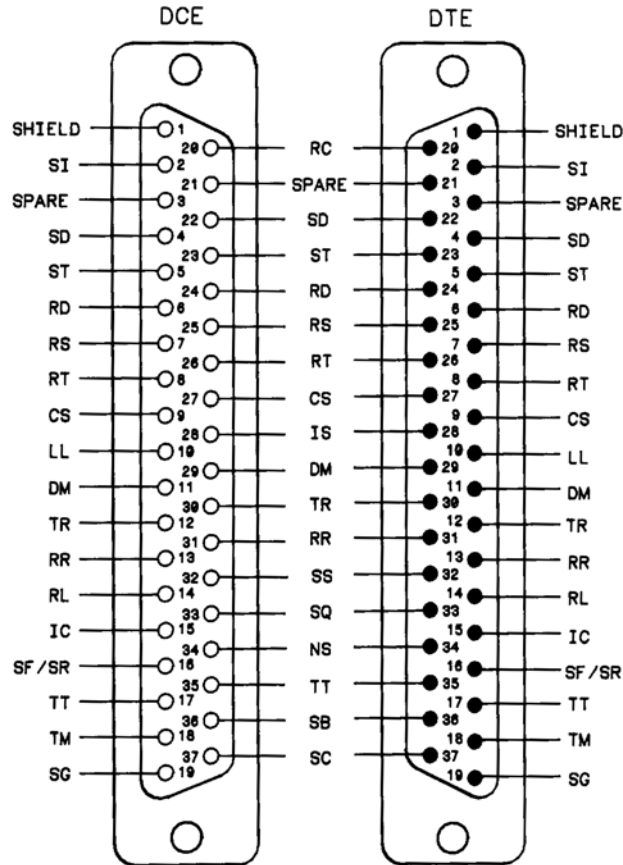


Figure 17: RS449 Connector with Pin Assignments

9.3.1 Electrical

The balanced electrical standard (RS422) for the new interface is too involved to present here without presenting virtually the entire standard. This is because the higher data rates used with these standards requires more involved specifications. The primary points are:

1. The signal voltage levels are less than $|6V|$ open circuit and less than $|3V|$ at nominal load.
2. The receiver should require a maximum differential voltage of 200 mV to assume the intended state over the common mode voltage range of $-7V$ to $+7V$. The receiver should operate with a maximum differential input of 12V.
3. The nominal impedance is 100Ω and the minimum load impedance is not less than 90Ω .
4. The input impedance of the receivers should be greater than $4K\Omega$.

5. The short circuit current is 150 mA.
6. The risetime of the data pulses is less than 0.1 x (bit period) when the bit period is greater than 200ns and less than 20ns when the bit period is less than 200ns.

The unbalanced electrical standard (RS423) is also too involved to present in this document and is only mentioned because many of the lines (Category 11) are operated unbalanced at all times. The characteristics for the unbalanced signals are much the same as for the balanced signals once the lack of the differential characteristic is taken into account. Consult the EIA Standard for further information.

PINS	DIRECTION		CIRCUIT	CATEGORY	DESCRIPTION
	DTE	DCE			
1		-	SHIELD	--	
2		←	SI	11	Signaling Rate Indicator
20		←	RC	11	Receive Common
		-	SPARE	--	
21		-	SPARE	--	
4	22	→	SD	1	Send Data
5	23	←	ST	1	Send Timing
6	24	←	RD	1	Receive Data
7	25	→	RS	1	Request to Send
8	26	←	RT	1	Receive Timing
9	27	←	CS	1	Clear to Send
10		→	LL	11	Local Loopback
28		→	IS	11	Terminal in Service
11	29	←	DM	1	Data Mode
12	30	→	TR	1	Terminal Ready
13	31	←	RR	1	Receiver Ready
14		→	RL	11	Remote Loopback
32		→	SS	11	Select Standby
15		←	IC	11	Incoming Call
33		←	SQ	11	Signal Quality
16		→	SF/SR	11	Select Frequency/
34		→	NS	11	New Signal
17	35	→	TT	1	Terminal Timing
18		←	TM	11	Test Mode
36		←	SB	11	Standby Indicator
19		→	SG	11	Signal Ground
37		→	SC	11	Send Common

Table 7: Interchange Circuits for RS449

10. IEEE1284 Overview

The standard printer or parallel port on IBM PC/AT[®]s has been the Centronics interface. Hewlett-Packard pioneered an extension of this interface to allow bi-directional

communication with printers and other parallel devices. This standard has been adopted by the IEEE and incorporated into a specification: *Parallel Peripheral Interface for Personal Computers, IEEE Std. 1284-1994*.

The standard identifies several types of bi-directional communications standards. The ALD-232A presently supports nibble and ECP modes. Nibble mode uses the status lines on the standard Centronics interface to send data back to the computer. ECP mode uses the data lines for bi-directional communications. Compatibility mode only moves data from the computer to the printer and utilizes the data lines as well.

The signals of the interface are redefined from the compatibility mode names when ECP or nibble mode is in use. The standard interface connector is a DB25 on the computer and a 36 pin 'blue ribbon' connector on the printer or peripheral. The ALD-232A provides a cable to intercept and monitor this bus by connecting through the DB25 connector. [The cable used is the same one as used by the RS232D interface.]

Centronics Signal name	Nibble Mode name	DB25 connector		Printer Connector		Source
		Signal	Return	Signal	Return	
nSTROBE	HostClk	1	18	1	19	Host
Data 0	Data 0	2	18	2	20	Host
Data 1	Data 1	3	19	3	21	Host
Data 2	Data 2	4	19	4	22	Host
Data 3	Data 3	5	20	5	23	Host
Data 4	Data 4	6	20	6	24	Host
Data 5	Data 5	7	21	7	25	Host
Data 6	Data 6	8	21	8	26	Host
Data 7	Data 7	9	22	9	27	Host
nACK	PtrClk	10	22	10	28	Printer
BUSY	PtrBusy	11	24	11	29	Printer
PAPER ERROR	AckDataReq	12	-	12	-	Printer
SELECT	Xflag	13	-	13	-	Printer
nAUTOFD	HostBusy	14	-	14	-	Host
nFAULT	nDataAvail	15	-	32	-	Printer
nINIT		16	25	31	30	Host
nSELECT IN	1284 Active	17	23	36	33	Host
CHASSIS GND	CHASSIS GND	-	-	17		-
SIGNAL GND	SIGNAL GND	-	-	16		-
+5V	+5V	-	-	35		Host

Table 8: Parallel Port Connections

Compatibility mode data simply places data on the data bus and pulses the STROBE. The host then either waits for BUSY to negate or looks for nACK to assert. Specific timing must be observed to conform with the specification.

Nibble mode provides one means of reverse data transfer (from the printer to the computer). This direction traffic requires that a nibble mode negotiation must take place between the printer and the computer. This negotiation involves the interlocking of various control and status signals on the bus. After the negotiation is complete, 2 4-bit nibbles are transferred back to the computer over 4 status lines. If the printer has more data, it may be transferred without re-negotiating nibble mode. The host may at any time return to standard Centronics mode [a.k.a. compatibility mode] by negating 1284 Active.

ECP (Extended Capabilities Port) mode provides an asynchronous, byte-wide, bi-directional channel. An interlocked handshake replaces compatibility mode's minimum timing requirements. A control line is provided to distinguish between command and data transfers. A command may optionally be used to indicate single byte data compression (run length encoding) or a channel address.

For a complete description of the operation of IEEE1284, the specification may be purchased from:

The Institute of Electrical and Electronics Engineers
345 East 47th St.
New York, NY 10017-2394
1- (800) 678-IEEE

11. Appendix B: Codes

11.1 ASCII Code

Hex	x0	x1	x2	x3	x4	x5	x6	x7	x8	x9	xA	xB	xC	xD	xE	xF
0x	NUL	SOH	STX	ETX	EOT	ENQ	ACK	BEL	BS	HT	LF	VT	FF	CR	SO	SI
1x	DLE	DC1	DC2	DC3	DC4	NAK	SYN	ETB	CAN	EM	SUB	ESC	FS	GS	RS	US
2x	SP	!	“	#	\$	%	&	‘	()	*	+	,	-	.	/
3x	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
4x	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
5x	P	Q	R	S	T	U	V	W	X	Y	Z	[\]	^	_
6x	`	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
7x	p	q	r	s	t	u	v	w	x	y	z	{		}	~	DEL

11.2 EBCDIC Code

Hex	x0	x1	x2	x3	x4	x5	x6	x7	x8	x9	xA	xB	xC	xD	xE	xF
0x	NUL	SOH	STX	ETX	PF	HT	LC	DEL	O8h	RLF	SMM	VT	FF	CR	S0	SI
1x	DLE	DC1	DC2	DC3	RES	NL	BS	IL	CAN	EM	CC	CU1	IFS	IGS	IRS	IUS
2x	DS	SOS	FS	23h	BYP	LF	ETB	ESC	28h	29h	SM	CU2	2Ch	ENQ	ACK	BEL
3x	30h	31h	SYN	33h	PN	RS	UC	EOT	38h	39h	3Ah	CU3	DC4	NAK	3Eh	SUB
4x	SP	41h	42h	43h	44h	45h	46h	47h	48h	49h	CNT	-	<	(+	
5x	&	51h	52h	53h	54h	55h	56h	57h	58h	59h	!	\$	*)	;	^
6x	_	/	62h	63h	64h	65h	66h	67h	68h	69h		‘	%	_	>	?
7x	70h	71h	72h	73h	74h	75h	76h	77h	78h	‘	:	#	@	‘	=	“
8x	80h	a	b	c	d	e	f	g	h	i	8Ah	8Bh	8Ch	8Dh	8Eh	8Fh
9x	90h	j	k	l	m	n	o	p	q	r	9Ah	9Bh	9Ch	9Dh	9Eh	9Fh
Ax	A0h	~	s	t	u	v	w	x	y	z	Aah	Abh	Ach	Adh	Aeh	Afh
Bx	B0h	B1h	B2h	B3h	B4h	B5h	B6h	B7h	B8h	B9h	Bah	BBh	BCh	BDh	Beh	BFh
Cx	{	A	B	C	D	E	F	G	H	I	Cah	CBh	CCh	CDh	CEh	CFh
Dx	}	J	K	L	M	N	O	P	Q	R	DAh	DBh	DCh	DDh	DEh	DFh
Ex	\	E1h	S	T	U	V	W	X	Y	Z	EAh	EBh	ECh	EDh	EEh	EFh
Fx	0	1	2	3	4	5	6	7	8	9	FAh	FBh	FCh	FDh	FEh	FFh

11.3 Transcode

HEX	0	1	2	3
0	SOH	&	-	0
1	A	J	/	1
2	B	K	S	2
3	C	L	T	3
4	D	M	U	4
5	E	N	V	5
6	F	O	W	6
7	G	P	X	7
8	H	Q	Y	8
9	I	R	Z	9
A	STX	SP	ESC	SYN
B	.	\$	'	#
C	<	*	%	@
D	BEL	US	ENQ	NAK
E	SUB	EOT	ETX	EM
F	ETB	DLE	HT	DEL

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