

USER GUIDE
ALD-488
IEEE-488
BUS ANALYSIS PROBE



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Introduction

The ALD-488 Analysis Probe Interface provides a complete interface between any IEEE-488 bus system and the following logic analyzers:

HP 1650A, HP 1650B, HP 1651B, HP 1652B, HP 1653B,
HP 1660A/61A/62A/63A, HP 16510A, HP 16510B, HP 16550A or Agilent 167xx.

The configuration software on the flexible disk sets up the format specification menu of the logic analyzer for compatibility with IEEE-488 bus systems. It also provides the inverse assembler for obtaining displays of the bus parameters.

CHAPTER 1 **Setting Up the ALD-488**

Introduction

This chapter explains how to install and configure the ALD-488 Analysis Probe Interface to perform IEEE-488 bus measurements with the supported logic analyzers.

Duplicating the Master Disk

Before you use the ALD-488 software, make a duplicate copy of the ALD-488 master disk. Then store the master disk and use the back-up copy to configure your logic analyzer. This will help prevent the possibility of losing or destroying the original files in the event the disk wears out, is damaged, or a file is accidentally deleted.

To make a duplicate copy, use the Duplicate Disk operation in the disk menu of your logic analyzer. For more information, refer to the reference manual for your logic analyzer.

Equipment Supplied

The ALD-488 Analysis Probe Interface consists of the following equipment:

- The analysis Probe interface hardware, which consists of the analysis Probe interface circuit card assembly.
- The configuration files and inverse assembler software on a 3.5-inch disk.
- This user's guide.

Minimum Equipment Required

The minimum hardware required for state or timing analysis of an IEEE-488 bus target system consists of the following:

- An HP 1650A, HP 1650B, HP 1651B, HP 1652B, HP 1653B, HP 1660A/61A/62A/63A, HP 16510A, HP 16510B, HP 16550A or Agilent 167xx Logic Analyzer.
- The ALD-488 IEEE-488 Bus Analysis Probe Interface.

Installation Overview

The following procedure describes the major steps required to perform measurements with the ALD-488 Analysis Probe Interface.

1. Connect the pod cable(s) from the logic analyzer to the ALD-488 Analysis Probe Interface Board as shown in table 1-1.
 - **NOTE:** The J1 and J2 connectors on the ALD-488 are identical.
2. Plug the ALD-488 PC board onto the IEEE-488 connector of the system being monitored. Secure the ALD-488 in place by tightening the two screws on the ALD-488 IEEE-488 connector.
3. Load the logic analyzer configuration and inverse assembler for the specified logic analyzer.
4. If you want timing analysis, configure the logic analyzer for timing analysis.

Connecting to the ALD-488

Connect the logic analyzer pods to the ALD-488 Analysis Probe Interface as listed in table 1-1. The numbers at the column tops refer to logic analyzer pods, while the designations in the boxes are ALD-488 connectors.

Table 1-1. Logic Analyzer Connections and Configuration Files

Logic Analyzer Pod	File	Pod 3	Pod 2	Pod 1
HP 1651B, HP 1653B, HP 1650A, HP 1650B, HP 16510A, HP 1652B, and HP 16510B	A488	--	J2	J1 clk ↓
HP 16550A, HP 1660A/61A/62A	B488	J2	--	J1 clk ↓
HP 1663A	B488		--	*J1 clk ↓

- * The HP 1663A Logic Analyzer can only look at state or timing; therefore, only one pod needs to be connected. Use the Configuration menu to select State or Timing.

Setting Up the Analyzer from the Disk

One disk supplied with your ALD-488. The contents are:

a488	DISK1.DAT
ald488_i	INDEX.TXT
b488	INFO.TXT

16500/166x Installation:

Copy the files *a488*, *b488* and *ald488_i* to the location on your hard disk where you keep your configurations (e.g. \\configs). Keep the diskette supplied with the ALD-488 in a safe location in case of damage or accidental erasure from the hard disk.

Next, load the configuration file, either *a488* or *b488* into the slot where your 16550 (or equivalent) card is located on your analyzer. DO NOT use “LOAD ALL”. This will result in the error message “SOME OR ALL CONFIGURATIONS NOT LOADED”. Next load the data format utility, *ald488_i*, as appropriate. After you have saved for the first time, it will not be necessary to load the format utility again.

16700 Installation

The screen format utilities must be ‘installed’ in the 16700 series analyzers. The disk is an ‘installable’ diskette. Insert the diskette into the analyzer’s floppy drive and invoke the ‘System Administrator Tools’ and the Software Install tab. Click the *Install* button. In the Media window, select the Flexible disk then click the *Apply* button. Select the package in the window and click the *Install* button. This will install the appropriate data formatter in the logic analyzer and configuration files.

After you have installed the ALD-488 diskette, a directory structure will be created on the logic analyzer: */logic/configs/ALD/ALD488.*

In this directory there will be 5 files:

IEEE488.__A	16550A Configuration
IEEE488.__B	16555A Configuration
IEEE488.__C	16712A Configuration
IEEE488.__D	16717A Configuration
IEEE488.__E	16752A Configuration

Choose the file appropriate to the logic analyzer board in your 167xx.

If the analyzer in your 167xx is not one of these types, attempt loading one of the configurations. The logic analyzer will attempt a conversion process. Some warnings may appear. Commonly a pod re-assignment message will identify how the pods on the conversion target should be connected in reference to the original configuration.

If the conversion is not successful, contact Advanced Logical Design, Inc.

Timing Analysis

The ALD-488 can also be used for timing analysis. The format specification loaded for state analysis is used for timing analysis.

For those logic analyzers which only use one pod (HP 1663A), load the configuration file as described above, then use the Type field in the Configuration menu and select Timing. You do not have to change connectors, since J1 and J2 are identical.

For those logic analyzers which use two pods, you can also configure the logic analyzer to display both state and timing together (Mixed Display). The state listing will be on Analyzer 1, and the timing display will be on Analyzer 2. To configure the logic analyzer for Mixed Display, use the Trace menu to set Count Time to On. You can then select Mixed Display.

CHAPTER 2 Analyzing the IEEE-488

Introduction

This chapter provides reference information on the format specification configured by the ALD-488 software. It also contains information about the inverse assembler and status encoding.

Format Specification

When you use the ALD-488 Analysis Probe Interface, the format specification will be set up by the flexible disk software similar to that shown in figure 2-1. There will be some slight differences in the display, according to which logic analyzer you are using. For example, some logic analyzers do not have a Clock Period field. Refer to your logic analyzer manual to see which fields and displays are available.

Table 3-1 in chapter 3 lists the IEEE-488 signals for the ALD-488 Analysis Probe Interface, and their corresponding lines to the logic analyzer.

- **NOTE** For those logic analyzers which have a Clock Period field (HP 1650A, HP 1650B, HP 1651B, HP 1652B, HP 1653B, HP 16510A, and HP 16510B), the Clock Period field should remain in the current selection (> 60 ns) for proper ALD-488 operation. For more information on the Clock Period field, refer to the reference manual for your logic analyzer.

Figure 2-1. Format Specification for IEEE-488

Label	Pol	15	87	0
ADDR	+		
DATA	-	*****	
STAT	+	*****	
CYCLE	-	**.....	
COMMND	-	*..*
REN	-	*.....	
IFC	-	*.....	
SRQ	-	*.....	

The Inverse Assembler

The ALD-488 inverse assembler is automatically loaded by loading the configuration file for the logic analyzer and bus system.

There is an Address (ADDR) label set up in the State Format Specification with no bits assigned to the label.

This label must be present when you are using an inverse assembler. If the ADDR label appears on screen, you can go to the State Display menu (State Listing menu in some logic analyzers) and move this label off the screen. This label is moved off the screen by the configuration file when the software is loaded.

IEEE-488 Analysis

The IEEE-488 Bus is a parallel bus with eight data lines, three handshake lines and five control lines. A brief overview of IEEE-488 is given in appendix A.

The function of the ALD-488 when monitoring the IEEE-488 Bus is to connect onto the bus, provide easy connection to the logic analyzer, set up the logic analyzer menus, and inverse assemble captured data.

The ALD-488 can monitor the state of all the IEEE-488 signal lines.

- **NOTE** The logic analyzer will flash "Warning Slow Clock" when data is no longer being transmitted across the bus. If you press STOP at this point, the end of the data stream will be displayed.

Status (STAT) Lines

The State Listing monitors the IEEE-488 interface management (ATN, EOI, REN, IFC, and SRQ) and handshake (NDAC, DAV, and NRFD) lines under the Status label. Only the interface management lines are used in the inverse assembler. Table 2-1 shows which IEEE-488 line corresponds to which Status line.

Table 2-1. Status Lines

Status Line	IEEE-488 Line	Status Line	IEEE-488 Line
STAT 0	ATN	STAT 5	SRQ
STAT 1	EOI	STAT 6	NDAC
STAT 2	REN	STAT 7	DAV
STAT 3	IFC	STAT 8	NRFD

Cycle Lines

The cycle lines are the IEEE-488 ATN and EOI lines and are the same as the first two STAT lines. They are displayed in the State Display (State Listing in some logic analyzers) in their symbol format.

Clocks

In state analysis the logic analyzer is clocked on the falling edge of the Valid (DAV) signal. DAV is brought out to the clock pin on both the ALD-488 "J1" and "J2" connectors.

CHAPTER 3

General Information

Analysis Probe Interface Characteristics

This chapter contains additional reference information including the characteristics and signal mapping for the ALD-488 Analysis Probe Interface.

- **Bus Compatibility:**
IEEE-488
- **Accessories Required:**
None
- **Signal Line Loading:**
With one pod cable connected:
DAV : 50 k Ω + 20pf
All Other Signals 100k Ω + 10pf
With one pod cable connected:
DAV : 25 k Ω + 40pf
All Other Signals 50k Ω + 20pf
- **Bus Signals Displayed:**
DI01 - 8, IFC, ATN, SRQ, REN, EOI, DAV, NRFD, NDAC.
- **Power Requirements:**
None

- **Logic Analyzer Required:**
HP 1650A, HP 1650B, HP 1651B, HP 1652B,
HP 1653B, HP 1660A/61A/62A/63A, HP 16510A, HP 16510B, HP 16511B, or HP 16550A
- **Number of Probes Used:**
One or two 16-channel probes

Bus Signal to ALD-488 Connector Mapping

Table 3-1 lists the IEEE-488 bus signals and the connections to the logic analyzer. Since J1 and J2 are identical, they can be interchanged.

Table 3-1. IEEE-488 Signal List

Logic Analyzer Bit (J1)	Logic Analyzer Bit (J2)	IEEE-488 Signal
JCLK	JCLK	DAV
0	0	DIO1
1	1	DIO2
2	2	DIO3
3	3	DIO4
4	4	DIO5
5	5	DIO6
6	6	DIO7
7	7	DIO8
8	8	ATN
9	9	EOI
10	10	REN
11	11	IFC
12	12	SRQ
13	13	NDAC
14	14	DAV
15	15	NRFD

APPENDIX A IEEE-488 Overview

Introduction

The following is a brief overview of IEEE-488. If additional information is needed, obtain the standard from the appropriate source.

The IEEE-488

The IEEE-488 employs a 16-line bus to interconnect up to 15 instruments. Each instrument on the bus is connected in parallel to the 16 lines of the bus. Eight of the lines are used to transmit data and the remaining eight are used for data transfer control (handshake) and bus management. Data is transferred by means of an interlocked "handshake," permitting asynchronous communication over a wide range of data rates.

The IEEE-488 structure is diagrammed in figure A-1. Four types of devices may be used on the bus based on their functions:

1. devices only able to talk;
2. devices only able to listen;
3. devices able to talk and listen;
4. devices able to talk, listen, and control.

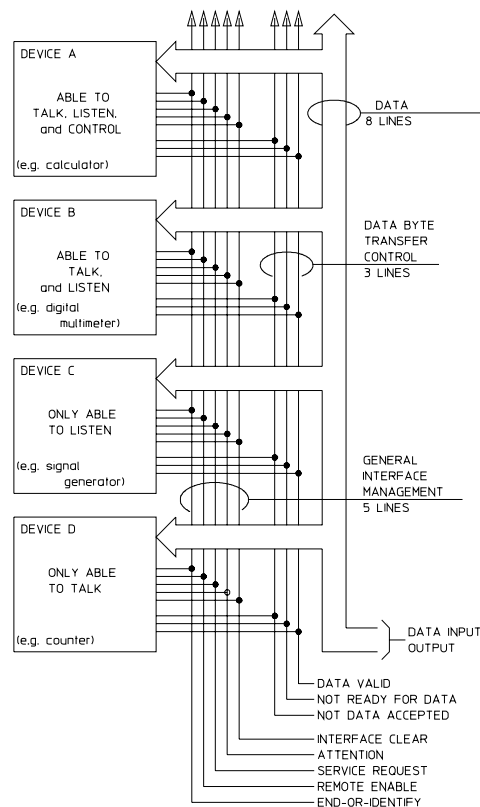
The simplest instrument is one that only talks. When signaled, this device enters its output on the data bus lines in a fixed configuration. The configuration may be altered only by front-panel control.

Devices that only listen respond to data from the IEEE-488 data lines. In the case of a signal generator, this data could cause the instrument to output signals of different amplitude and frequency, external to the bus. Printers are frequently listen-only instruments.

A digital multimeter is a device that listens and talks. The multimeter is configured by signals from the controller, takes the requested reading, and returns the results on the bus. The controller, along with talk and listen capabilities, controls all operations on the interface bus.

As shown in figure A-1, the 16 lines of the IEEE-488 form three functional groups: five lines for interface management, three lines for handshake (data byte transfer) control, and eight bi-directional lines for carrying data.

Figure A-1. IEEE-488 Bus and interface Capabilities



Interface Management Lines

1. Attention (ATN) specifies how and by which devices data on the data input/output (DIO) lines is to be interpreted. ATN is pulled low for commands (Command Mode) and released for data by the controller.

In command mode the controller is active and all other devices are waiting for instructions. Command Mode instructions which can be issued by the controller fall into five groups:

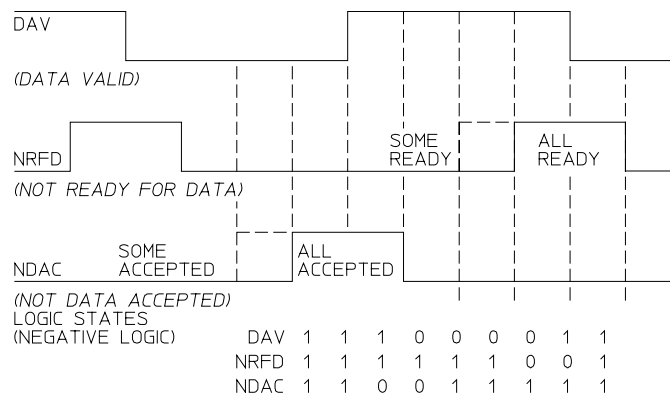
- a. Talker Address Group (TAG) commands enable a specific device to talk. Only one device at a time may act as the talker. When the controller addresses one device to talk, the previous talker is automatically unaddressed and ceases to be a talker.
 - b. Listener Address Group (LAG) commands enable a specific device to listen. Up to 14 devices at a time may be listeners.
 - c. Universal Command Group (UCG) commands cause all bus devices capable of responding to these commands from the controller to do so at any time regardless of whether they are addressed.
 - d. Addressed Command Group (ACG) commands are similar to universal commands except that they are recognized only by devices that are addressed as listeners only.
 - e. Secondary Command Group (SCG) commands are used when addressing extended listeners and talkers, or enabling the parallel poll.
2. Interface Clear (IFC) puts the entire system into a predefined quiescent state.
 3. Service Request (SRQ) is used by a device to indicate a need for attention and to request an interruption of the current sequence of events.
 4. Remote Enable (REN), in conjunction with other messages, selects between alternate sources of device programming data (typically IEEE-488 vs front panel).
 5. End or Identify (EOI) indicates the end of a multiple-byte transfer sequence, or with ATN executes a polling sequence.
- The Unlisten Address Command (UNL) unaddresses all listeners that have been previously addressed to listen. The Untalk Address Command (UNT) unaddresses any talker that has been previously addressed to talk.

Handshake Lines

1. Data Valid (DAV) indicates the availability and validity of information on the data lines.
2. Not Ready For Data (NRFD) indicates the state of readiness of devices to accept data.
3. Not Data Accepted (NDAC) indicates the condition of acceptance of data by device(s).

The DAV, NRFD, and NDAC lines operate in a three-wire interlocked handshake process to transfer each data byte across an interface (see figure A-2).

Figure A-2. IEEE-488 Handshake Sequence



A handshake sequence is entered with the listener-controlled NRFD and NDAC both low. Line DAV is high. As each listener is ready to accept data, it releases its Not Ready For Data (NRFD) line. When all listeners have released their NRFD line, pull-up resistors on the line pull NRFD high. The talker signals new Data Valid by pulling the DAV line low. Listeners respond by pulling their NRFD outputs low. During the period that

listeners accept data, they release the Not Data Accepted (NDAC) line. When data has been accepted by all the listeners, the NDAC line goes high. Acknowledgment by the talker releases the DAV line, and the handshake is completed by the listeners by pulling the NDAC low. A legal handshake must proceed in the manner shown in figure A-2. Note that the NRFD and NDAC lines may never go high (logic 0) together.

APPENDIX B

Troubleshooting

If you encounter difficulties while making measurements, use this section to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions. Error messages which may appear on the logic analyzer are listed below in quotes ". Symptoms are listed without quotes.

If you are still having difficulties after trying the suggestions below, please contact Advanced Logical Design for additional assistance.

"No Configuration File Loaded"

Verify that the appropriate module has been selected from the Load {module} from File {filename} in the HP 16500 disk operation menu. Selecting Load {All} will cause incorrect operation when loading most analysis probe interface configuration files.

"Selected File is Incompatible"

The logic analyzer displays this message if you try to load a configuration file for the wrong module. Ensure that you are loading an ALD-488 configuration file.

". . . Inverse Assembler Not Found"

This error occurs if you rename or delete the inverse assembler file that is attached to the configuration file. Ensure that the inverse assembler file is not renamed or deleted.

Incorrect Inverse Assembly

This problem is usually caused by a hardware problem in the target system. A locked status line will often cause incorrect or incomplete inverse assembly.

- Check the activity indicators for status lines locked in a high or low state.
- Verify that the STAT, DATA, and ADDR format labels have not been modified from their default values. These labels must remain as they are configured by the configuration file.
- Verify that storage qualification has not excluded storage of all the needed opcodes and operands.
- Verify that the "Invasm" field has been selected in the Listing menu under the Data field.

No Activity on Activity Indicators

If there is no activity, one of the cables, board connections, or analysis probe interface connections is probably loose. Check all connections.

Capacitive Loading

Excessive capacitive loading can cause signals to degrade, resulting in incorrect capture by the analysis probe interface or system lockup in the microprocessor. All analysis probe interfaces add additional capacitive loading.

"State Clock Violates Overdrive Specification"

At least one 16-channel pod in the state analysis measurement stored a different number of states before trigger than the other pods. This is usually caused by sending a clocking signal to the state analyzer that does not meet all of the specified conditions, such as minimum period, minimum pulse width, or minimum amplitude. Poor pulse shaping could also cause this problem.

- **NOTE** The error message "State Clock Violates Overdrive Specification" should only occur for HP 1650A,B, HP 1652B, and HP 16510A,B Logic Analyzers with the Clock Period field set to <<60 ns. If this error message is observed with the Clock Period set to >>60 ns, you may have a faulty logic analyzer. If a failure is suspected in your logic analyzer, contact your nearest Hewlett Packard Sales/Service Office for information on servicing the instrument.

"Waiting for Trigger"

If a trigger pattern is specified, this message indicates that the specified trigger pattern did not occur. Verify that the triggering pattern is correctly set.

If a "don't care" trigger condition is set, this message indicates:

- For an HP 1650A,B, HP 1652B, or HP 16510A,B Logic Analyzer, the pattern duration is probably set to less than (<<) instead of greater than (>>). Since a "don't care" pattern is always true, the "less than" condition is never satisfied. Set the trace menu correctly for the measurement that is desired.

Intermittent Data Errors

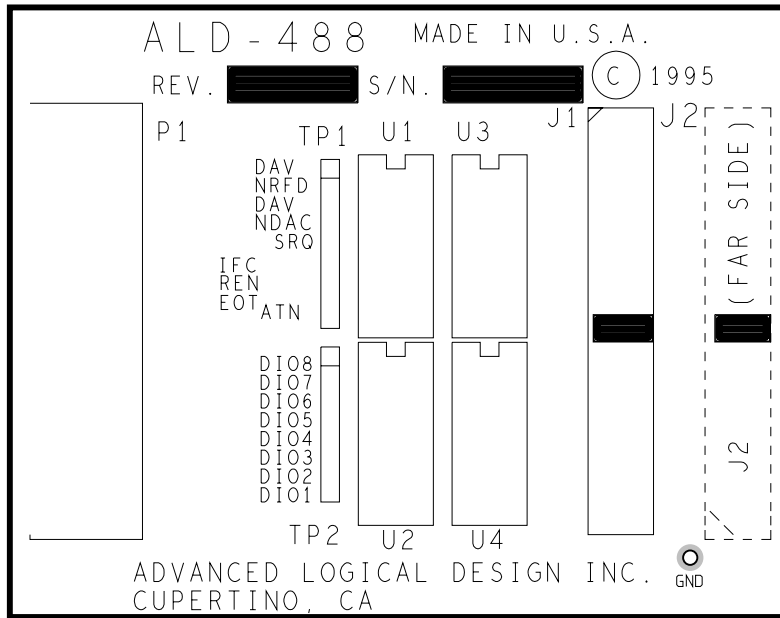
This problem is usually caused by incorrect signal levels. Adjust the threshold level of the data pod. Use an oscilloscope to check the signal integrity of the data lines, as needed.

Bent Pins

Bent pins on the analysis probe interface, pin protectors, or adapters can cause system errors or inverse assembly errors. Ensure all pins are properly aligned and making contact.

"Time from Arm Greater Than 41.93 ms."

The state/timing analyzers have a counter to keep track of the time from when an analyzer is armed to when it triggers. The width and clock rate of this counter allow it to count for up to 41.93 ms before it overflows. Once the counter has overflowed, the system does not have the data it needs to calculate the time between module triggers. The system must know this time to be able to display data from multiple modules on a single screen.



Rev B

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