USER GUIDE
CAN OPTION
FOR THE ALD-232A
BUS ANALYSIS PROBE
(Addendum to ALD-232A Manual)

advanced
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1. Introduction

The CAN option for the ALD-232-CAN analysis probe allows users to examine the operation of a CAN bus without having to manually decipher the serial protocol for the bus. The ALD-232-CAN analysis probe will display the data on the bus in an easy to read byte format.

1.1. Specifications

- Bus Loading: Standard CAN bus transceiver load.
- Probe Cable length: 24 in
- Connectors: 1 Male and 1 Female DB9 connector
- Power Required: ~325 mA supplied by the logic analyzer
- Mechanical: 4.0” x 7.5" x 2.0"
- Signals supported: CAN_H and CAN_L.
- Bus Speed: 10, 20, 50, 100, 125, 250, 500, 800 kBits/s and 1 Mbits/s

1.2. Logic Analyzers Supported

The CAN bus analysis probe may be used with all currently available 165XX and 167XX-system state analyzer modules, or with the 1660- or 1670-series logic analyzers. Two 17-channel pods are required.

1.3. Installing the Software

The installation process is different depending upon the Agilent analyzer model. The disk contains the following files:

DISK1.DAT	CANSTATE.__B	CANTIMING.__B
INDEX.TXT	IAACAN.I	
INFO.TXT		

167xx Models:
Insert the diskette included with this option into the 167xx floppy drive. Navigate to the ***System Administrator Tools*** tab of the analyzer. Select the ***Software Install*** tab. Next select the ***Install***… feature. Under ***Media***, choose ***Flexible Disk*** and then ***Appl***y. In the ***Flexible Disk Packages*** window, select the ALD-232-CAN package and click on ***Install***. This will load both the data formatter and the configurations.

165xx Models:
On these older model analyzers, files are copied onto the analyzer's hard disk. From the diskette supplied, copy the files from the right column on the previous page [CANSTATE, CANTIMING and IAACAN.I] to an appropriate place on the 16500, 166x or 167x hard drive.
After installing the software onto your analyzer, we recommend that you make duplicate disks and store the original supplied diskette in a safe location in case of problems that may arise with your analyzer at a future point in time.

1.4. Equipment Supplied

- RS232D, RS449, and IEEE 1284 and CAN Bus Analysis Probe
- This User Guide
- Diskettes including configuration files and screen data formatter
- 2 flat ribbon 'Y' Cable for connecting to the target bus for RS232, RS449 and IEEE1284
- CAN POD with two 9-pin D-Sub connectors, one male and one female, and an attachment cable to connect the POD to the ALD-232 box.

1.5. Minimum Equipment Required

In addition to the equipment supplied above, an Agilent analyzer is required.

2. Installation

The ALD-232-CAN is easy to install. The unit is simply connected between the logic analyzer and the CAN target and the supplied configuration is loaded into the logic analyzer.

2.1. Initial Inspection

Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until the contents of the shipment have been inspected mechanically and electrically. If the contents are incomplete, if there is mechanical damage or defect, or if the instrument does not operate, notify Advanced Logical design, Inc.. If the shipping container is damaged, or the cushioning materials show signs of stress, notify the carrier as well as the ALD office. Keep the shipping materials for inspection by the carrier.

2.2. Connection to the Logic Analyzer

The ALD-232-CAN both derives its power from the logic analyzer and provides it data through the pod connection cables. Both pods 1 and 3 should be connected. Note that Pod 2 is not used. The pod cables from the logic analyzer are plugged directly into the right side of the ALD-232. No additional terminators or adapters are required.

2.3. Connection to the CAN Bus

The ALD-232-CAN has several connectors on the top of the unit that allow it to be attached to several busses. The connector used for the CAN bus is the one identified as 'J2'. A short cable is supplied with a mating 26 pin IDC connector on one end and the other end has the CAN POD. The CAN POD has two 9-pin D-Sub connectors, one male and one female, to connect to the CAN bus.

Both 9-pin D-Sub connectors are wired the same, and form a straight-through connection for the CAN bus on all 9 pins. The pin-out of the connectors is shown in the table below, and conforms to the CiA Draft Standard 102 Version 2.0 (See Table 1).

Pin	Signal
1	Reserved
2	CAN_L (dominant low)
3	CAN_GND (Ground reference)
4	Reserved
5	CAN_SHIELD (optional CAN shield)
6	GND (optional CAN ground)
7	CAN_H (dominant high)
8	Reserved
9	CAN_V+ (optional CAN external power supply)

Table 1 – Singnals of the CAN 9-Pin D connector

The CAN POD has a small recessed slide switch on the side of the POD labeled 'COMMON' and 'ISOLATE'. In the COMMON position the GNDs for both sides of the opto-couplers in the POD are connected together, and power for the CAN transceiver is derived from the ALD-232-CAN unit. This is the shipping default.

In the 'ISOLATE' position the GNDs are not connected, and power for the bus side of the opto-couplers and the transceiver must be supplied by the CAN bus. The power must be supplied between pin 9 (CAN_V+) and pin 3 (CAN_GND). In the 'ISOLATE' mode there is a 1M ohm impedance between the two GNDs.

2.4. Loading The Software

The software should be installed onto the logic analyzer as described in section 1.2. Loading the analyzer again differs between the 16500 and 16700 series analyzers.

16700 Analyzers
After the software has been installed, a new inverse assembler (IAACAN) can be found in the /logic/ia directory. In addition a new directory will be created on your analyzer:

`/logic/configs/ALD/ALD232A_CAN`

In this directory will be 10 configuration files:

CANSTATE.__A	CANTIMING.__A	16550A Configuration Files
CANSTATE.__B	CANTIMING.__B	16555A Configuration File
CANSTATE.__C	CANTIMING.__C	16712A Configuration File
CANSTATE.__D	CANTIMING.__D	16717A Configuration File
CANSTATE.__E	CANTIMING.__E	16752A Configuration File

Load the configuration appropriate to the logic analyzer that you wish to use. The CANSTATE configurations are state setups using the inverse assembler, while the

CANTIMING configurations can be used to inspect the CAN line after going through the transceiver and opto-coupler.

16500 Analyzers

From the directory that you copied the 16500 CAN files, you may load a state only display, CANSTATE._B. This display is similar to the displays for the 16700 series analyzers, with the exception that it lacks the color and filter capabilities.

When loading this configuration, be sure to load only the slot that contains your logic analyzer. The default is to load ALL which will generate the message:

"**ONE OR MORE CONFIGURATIONS NOT LOADED**"

This means that the equipment loaded into your other slots have not been configured. The native logic analyzer for these configurations is the 16550. If you have another analyzer, the 16500 will attempt to convert the configuration for the installed analyzer.

The other file provided, IAACAN.I is an 'inverse assembler' file and is used to format the state data.

It should be noted, that some options shown in this manual are only available with the 16700 series analyzer (e.g. color coding and filtering).

2.5. POD Configuration

The POD configuration for all the supplied configurations sets up the logic analyzer pods 1 and 3 as follows (See Table 2):

MASTER CLOCK: J1↑
CLOCK QUALIFIER: L=1

NAME	POD 3 CHAN	POD 1 CHAN
DATA		15:0
STAT	13:0	
ADDR	15:14	
CANSHIFT		15:0
CLKSTB		CLK
FRMCOUNT	7:0	
CODE	10:8	
IDE		2
INFRAME	13	
CLKCAN	14	
CAN	15	
DATASTB	CLK	
SID		14:4
EID1		14:4,1:0
EID2		15:0

Table 2 – POD Configuration for CAN

When looking at CAN in timing mode, the internally derived clock 'CLKCAN' can be used as a guide to help with bit delineation. It should be kept in mind, though, that the CAN signal is the raw signal, while CLKCAN has been processed by the internal sampling clock, and therefore can have 100-200 nsec of delay. It should still be possible to use the rising edge of CLKCAN to see how the ALD-232-CAN interprets the data.

3. Operational Overview

Immediately after power is applied or **RESET** is depressed, the ALD-232-CAN will enter self-test mode. After the self-test is completed, the ALD-232-CAN will enter the RUN mode, with the interface connection (J1, J2 or J3) that was last used. [The first time the ALD-232-CAN is used, it will come up running in the CAN mode with the bit rate set to 1 Mb/sec]. The LED opposite the appropriate connector will be lit.

All operations of the ALD-232A are controlled by the keyboard. When the logic analyzer cables are plugged into the ALD232A, the unit will power up in the mode it was last in. Navigation through the options is very simple. An arrow (->) will point to the item that can be changed. A new value may be selected for that item by scrolling through the choices with the ◀ and the ▶ keys (See Figure 1). To move to a different item, use the ▲ and ▼ keys. The item at the top of the screen is the type of analysis desired [RS232 ASYNC, RS232 SYNC, RS449 ASYNC, RS449 SYNC, IEEE 1284 and CAN]. The last screen in the sequence is an informational screen.

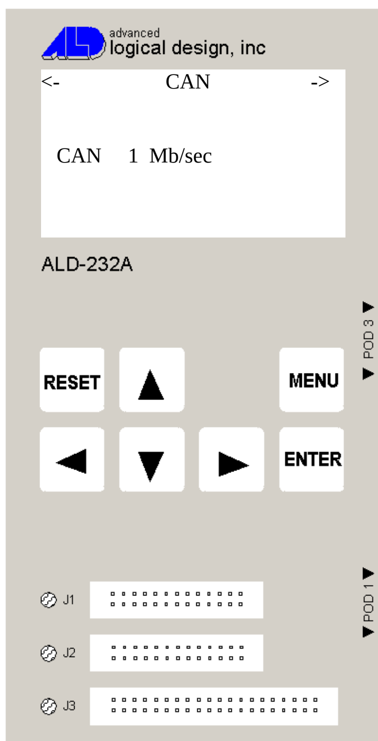

Figure 1: ALD-232-CAN Top Panel

The operation of the ALD-232-CAN in modes other than CAN is explained in the basic ALD-232 manual, also enclosed. This addendum covers only the CAN operation.

4. Analyzing CAN

The CAN Bus has been adopted for many automotive and industrial applications. It is a two-wire differential serial bus with a non-collision priority arbitration mechanism. It is used for many low speed applications (up to 1 Mbs). The ALD-232-CAN conforms to the protocol described in the CAN Specification Version 2.0, by Robert Bosch GmbH. The ALD-232-CAN supports all bit rates suggested in the CiA Draft Standard 102 version 2.0 (10, 20, 50, 100, 125, 250, 500, 800 kBits/s and 1 Mbits/s).

4.1. Run Time Display

When the analysis probe is running a CAN measurement, the unit's display will show the following information:

```
           CAN

-> CAN    1  Mb/sec
```

Figure 2 – Changing CAN transfer rate

This indicates that the CAN measurement is being done at 1 Mb/sec. To change the transfer rate use the ▼ to move the selection arrow (->) down to the second line where the CAN rate is displayed (See Figure 2). Then change the transfer rate by using the ◀ and the ▶ keys it is possible to cycle through all the possible rates. The new rate takes effect immediately after the change has been made.

4.2. Logic Analyzer Connections

The configurations shipped from the factory uses the following FORMAT setup with the fields necessary for the inverse assembler (See Figure 3).

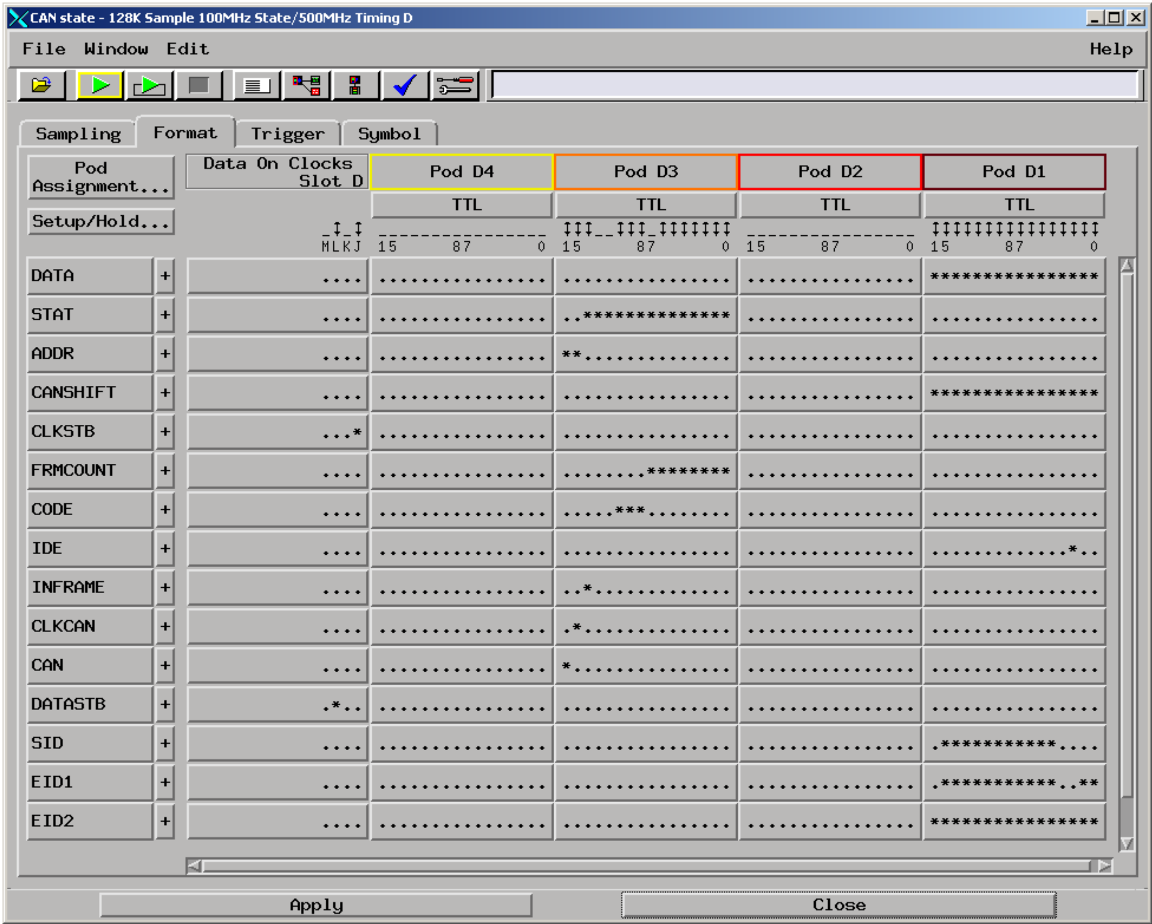

Figure 3 – Factory set up for Inverse Assembler

DATA	Field needed by the inverse assembler. It is a duplication of the internal 16-bit shift register (CANSHIFT).
STAT	Field needed by the inverse assembler. Is a combination of CODE and FRMCOUNT.
ADDR	Field needed by the inverse assembler. It is not used by the CAN inverse assembler and is set to two arbitrary bits.
CANSHIFT	This is a 16 bit shift register collecting the un-stuffed bits. It is presented to the logic analyzer with a DATASTB and a corresponding CODE, indicating the type of data held by the shift register.
CLKSTB	This is a qualified clock, which has a negative edge for each valid bit in a frame. Stuffed bits do not have a corresponding clock edge. This signal is used as the clock for the logic analyzer in state mode.
FRMCOUNT	This counter is started when a new frame has been detected, and increments for each valid bit in the frame.

CODE	This is a three bit code, which tells the inverse assembler what type of data is being presented at the time of DATASTB. For a list of the codes please see Table 3.
IDE	At the DATASTB signifying the first part of the address, this bit indicates whether we have a STANDARD ID or the first 11 bits of the EXTENDED ID.
INFRAME	This is an internal signal, which is set when the beginning of a frame is detected, and reset at the end of the frame. It can be used as a guide when inspecting the CAN line in timing mode.
CLKCAN	This is the internal clock, which is used to clock the CAN input signal. It can be used as a guide when inspecting the CAN line in timing mode.
CAN	This is the CAN signal after being processed by the CAN transceiver and opto-coupler. It can be used to inspect the CAN signal in timing mode.
DATASTB	This signal indicates to the logic analyzer, that the shift register contains information of interest to the inverse assembler. The CODE tells the inverse assembler, what kind of information is being presented.
SID	The part of the shift register holding the Standard ID, when the correct CODE is presented and the IDE bit is zero.
EID1	The part of the shift register holding the first 11 bits of the EXTENDED ID, when the correct CODE is presented and the IDE bit is one.
EID2	The part of the shift register holding the second 16 bits of the EXTENDED ID, when the correct CODE is presented.

The values for the CODE field are shown in the following table.

CODE	Data presented
0	End of frame
1	First part of ID
2	Second part of Extended ID
3	DLC
4	Data
5	CRC
6	Not used
7	Error Frame

Table 3 – Codes for presented data

4.3. State Analysis

4.3.1. Data collection

The ALD-232-CAN is primarily intended for state analysis of the CAN bus. Both POD 1 and POD 3 are used for the measurement. The analysis probe accumulates serial data into an internal 16-bit shift register and presents the data to the analyzer at key times of the frame, along with a code to indicate the meaning of the data.

4.3.2. Choosing Logic Analyzer Display

The configuration files supplied with the ALD-232-CAN option for the 16700 series logic analyzers are either for state analysis or for timing analysis. The 'as shipped' configuration for the trigger is set to trigger on any frames. The user may create any triggering situation appropriate to the problem being solved.

16500 users have 2 configurations to choose from, a state only and a timing only configuration. The POD connections for the two configurations are the same; the main difference between the configurations is the setting of the sampling mode.

The user can select the level of detail desired on the 16700 state display. This is accomplished using the **`Invasm>Filter`** option of the analyzer (See Figure 4). In addition, the colors of the different fields can be changed in the same menu (See Figure 5). Some of these options are shown below:

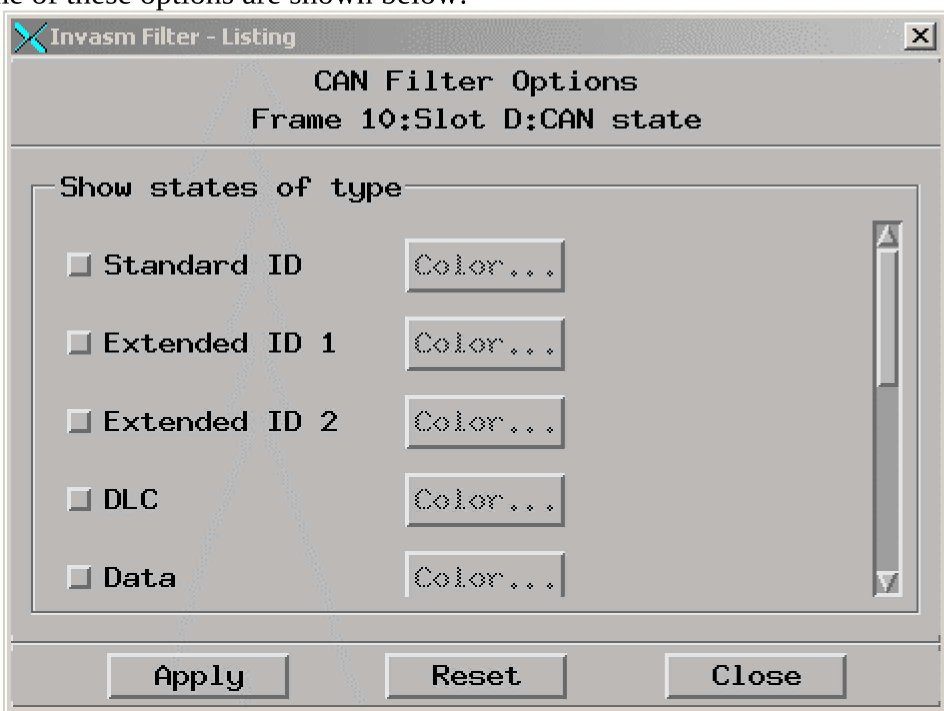

Figure 4 – CAN Filter Options window (features disabled)

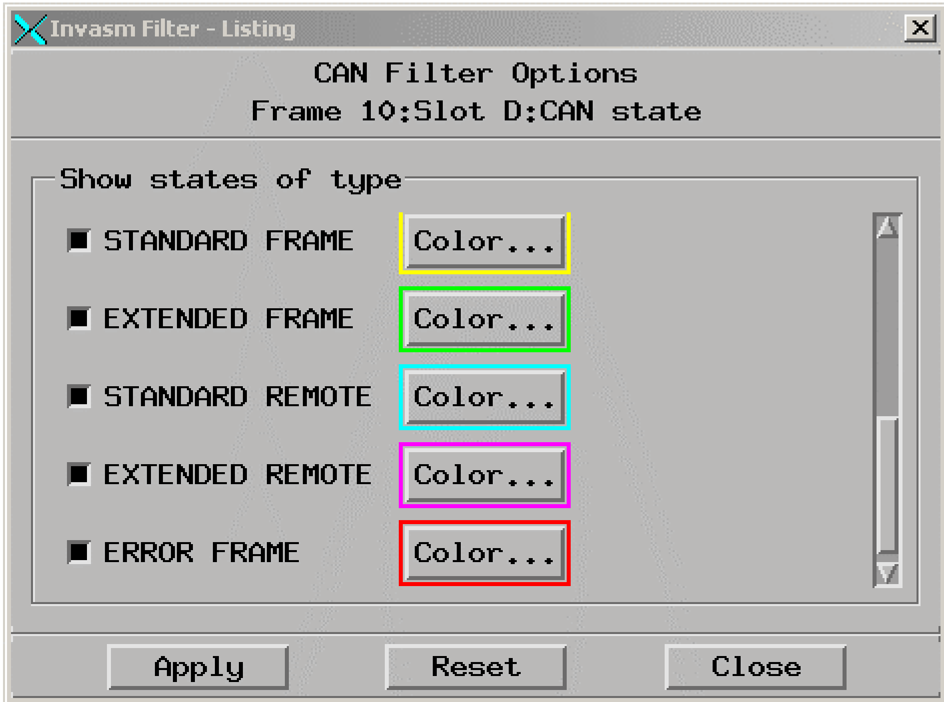

Figure 5 – CAN Filter Options window (features enabled)

The default in the 'as shipped' configurations is to have low level detail turned off and higher level assembled frames turned on.

These options are not available on the 16500, so all details are always shown, and in white only.

Below is an example of a display of captured frames, with only the high level frames shown, as assembled by the inverse assembler (See Figure 6). Notice how the different frame types are displayed in different colors. The field 'CAN_ID' is generated by the inverse assembler, and shows the complete CAN ID.

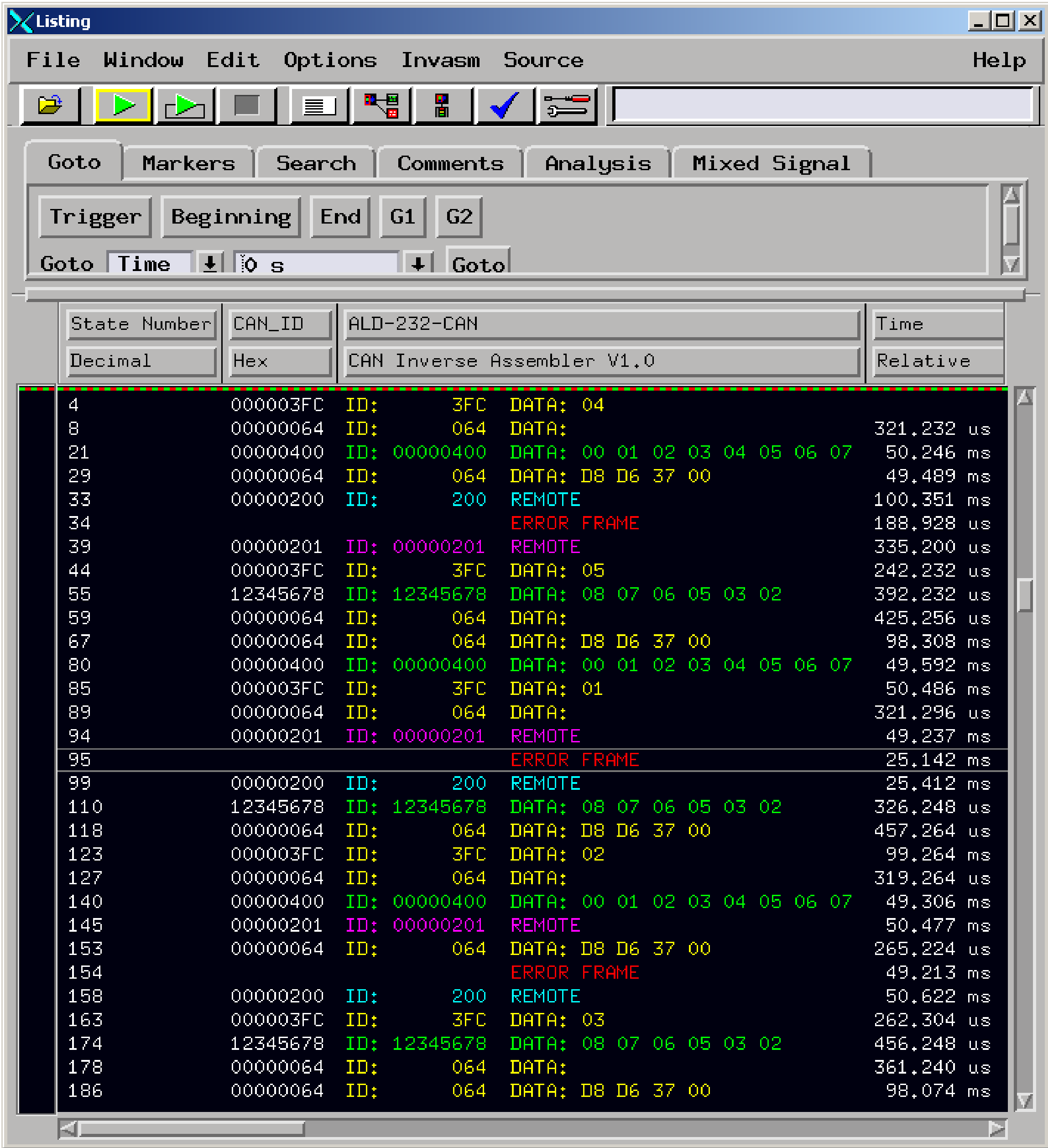

Figure 6 – High Level Frames Captured

The next example shows a display of captured frames, where all filters are turned on, showing all details. Here all the details are shown in white (See Figure 7). This shows the actual data captured by the logic analyzer at each of the field boundary events in the frame, where the ALD-232-CAN presents the data and generates a strobe. The significant events are:

SID is the Standard ID
EID1 is the first 13 bits of the Extended ID.
EID2 is the last 16 bits of the Extended ID.
DLC is the Data Length Code.

DATA is each data byte.
CRC is the CRC.

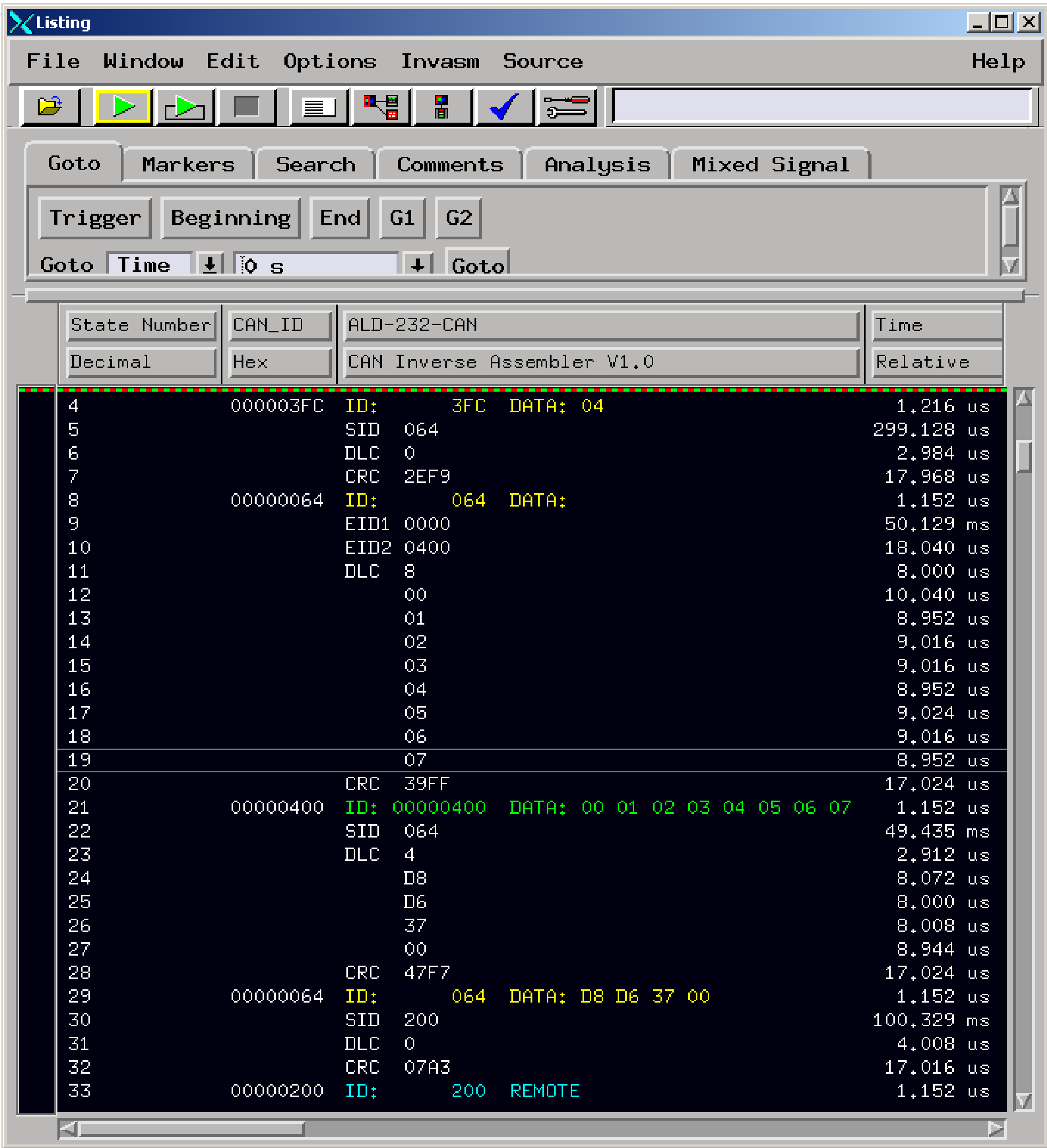

Figure 7 – Display of All Leveled Frames Captured

The display on a 16500 analyzer will be similar to the above capture, but without the colors.

4.4. Timing Analysis

The CAN signal is presented to the logic analyzer directly on Pod 3 and may be used to view the signal timing directly in timing mode.

In addition to the basic CAN signal, the analysis probe also presents some additional signals that can assist in interpreting the timing display. These are the signals use by the analyzer in state mode, and consist of the outputs from the internal state machine, that is used to decode the frame.

The signals generated by the FPGA can be display along with the CAN signal to help identify bit timing, stuff bits, fields, and frame boundaries. It should be noted that since the CAN signal is fed directly through the FPGA, while the state machine signals are internally clocked, there will be a skew between the CAN signal and the internally derived signals. This skew is around half a clock (CLKCAN).

See Figure 8 for an example with an explanation of some of the signals.

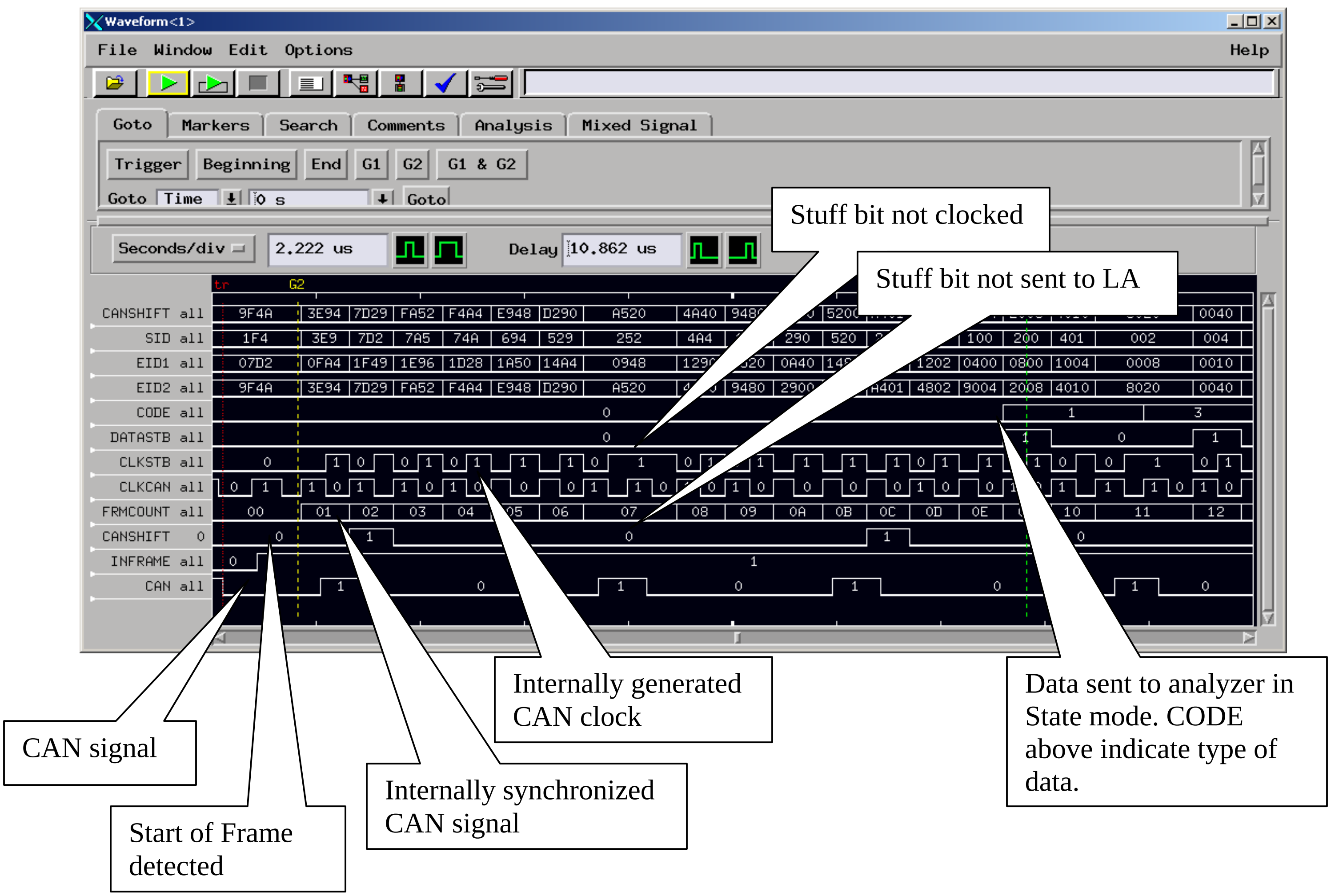

Figure 8 – Explanation of signals

5. Theory of Operation

The block diagram of the ALD-232-CAN analysis probe is shown below (See Figure 9):

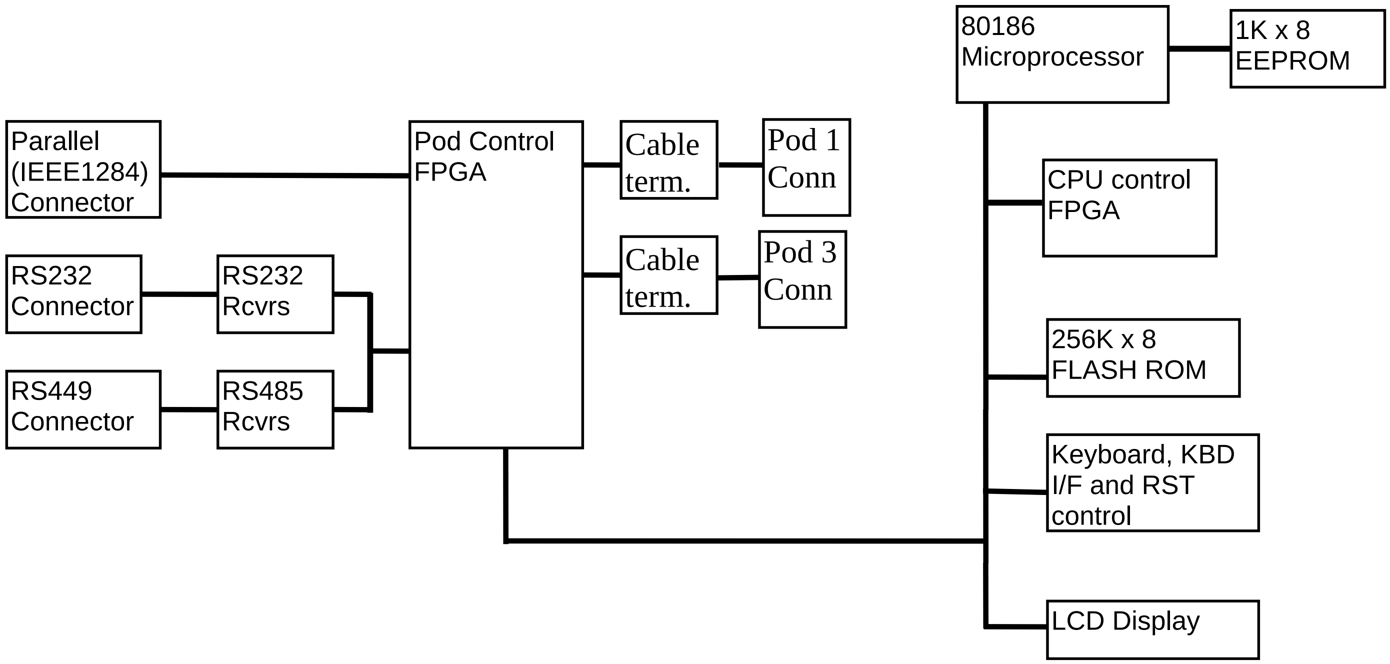

Figure 9 – Operation of 232A-CAN

The ALD-232-CAN is a complete small processor system, with RAM, ROM, keyboard and display and a data capture system. The microprocessor system downloads the FPGAs with code appropriate to the operation selected, and receives parametric data from the user to program both FPGAs.

The 80186 microprocessor system is conventional in design with the processor running at 32 MHz. Each time that the user selects a new parameter or option, that selection is recorded in the EEPROM. Data is also stored in the EEPROM after any mode change persists for more than 5 secs. This allows that selection to survive power loss. The Flash PROM contains not only the operational code, but also binary images of the code in both FPGAs. The CPU Control FPGA is downloaded automatically from the FPROM prior to the release of RESET from the 186. The Pod Control FPGA is downloaded under program control with code for RS232, RS449, IEEE1284, I^2C or CAN or any option that may be included.

The Pod Control FPGA collects data from the appropriate interface, RS232, RS449, IEEE1284 or and presents it to the pins of the logic analyzer. The FPGA acts as a dual UART or USRT.

In CAN mode, the CAN signal from the CAN interface pod is connected via the parallel (J1) port connector to the FPGA for processing. This FPGA contains all of the necessary logic to process the CAN signal, decoding the frame and presented it to the logic analyzer.

The FPGA directly generates the signals that are sent to the logic analyzer's Pod 1 and Pod 3.

Revision B

Advanced Logical Design, Inc.
12280 Saratoga-Sunnyvale Road. Suite 201
Saratoga, CA 95070
Voice: (408)446-1004
Fax: (408)446-1079
email: techsup@ald.com
URL: http://www.ald.com