

**USER GUIDE**  
**I<sup>2</sup>C OPTION**  
**FOR THE ALD-232A**  
**BUS ANALYSIS PROBE**  
(Addendum to ALD-232A Manual)



advanced  
logical design, inc.

## ***Limited Warranty***

This Advanced Logical Design product has a warranty against defects in material and workmanship for a period of 1 year from date of shipment. During warranty period, Advanced Logical Design, Incorporated will, at its option, either repair or replace products that prove to be defective.

For warranty service or repair, this product must be returned to Advanced Logical Design.

The Buyer shall prepay shipping charges to Advanced Logical Design and Advanced Logical Design shall pay shipping charges to return the product to the Buyer. However, the Buyer shall pay all shipping charges, duties, and taxes for products returned to Advanced Logical Design from another country.

Advanced Logical Design does not warrant that the operation of the instrument, software, or firmware will be uninterrupted or error-free.

# Table of Contents

1.	Introduction.....	4
1.1.	Specifications.....	4
1.2.	Features.....	4
1.3.	Logic Analyzers Supported.....	5
1.4.	Installing the Software.....	5
1.5.	Equipment Supplied.....	5
1.6.	Minimum Equipment Required.....	5
2.	Installation.....	6
2.1.	Initial Inspection.....	6
2.2.	Connection to the Logic Analyzer.....	6
2.3.	Connection to the Bus.....	6
2.4.	Loading The Software.....	7
2.4.1.	State Only Configuration.....	8
2.4.2.	Mixed Configuration.....	8
3.	Operational Overview.....	9
4.	Analyzing I <sup>2</sup> C.....	10
4.1.	Setting Threshold Voltage.....	10
4.2.	Run Time Display.....	10
4.3.	Logic Analyzer Connections.....	11
4.4.	State Analysis.....	11
4.4.1.	Choosing Logic Analyzer Display.....	11
4.4.2.	Interpreting the Display.....	16
4.5.	Timing Analysis.....	24
5.	Theory of Operation.....	26

# 1. Introduction

The I<sup>2</sup>C option for the ALD-232-I2C analysis probe allows users to examine the operation of an I<sup>2</sup>C bus without having to manually decipher the serial protocol for the bus. The ALD-232-I2C analysis probe will display the data on the bus in an easy to read byte format.

## 1.1. Specifications

- Bus Loading: 20kΩ shunted by 30 pF (at probe tip)
- Probe Cable length: 15 in
- Connectors: female 0.025" square post
- Power Required: ~325 mA supplied by the logic analyzer
- Mechanical: 4.0" x 7.5" x 2.0"
- Signals supported: SDA and SCL.
- Skew: skew due to signal buffering less than 10ns
- Max Delay (SCL,SDA) 22 ns
- Bus Speed: Both 100 KHz. and 400 KHz. speeds

## 1.2. Features

- I<sup>2</sup>C bus serial information is displayed as parallel bytes in state mode
- Two alternate display modes provide detail or overview of bus transactions
- Quickly determine the information content of I<sup>2</sup>C transactions
- Operates at low voltage with user-defined threshold levels of 0.5V to 3.0V
- View details of I<sup>2</sup>C bus timing with signal pass-through mode
- View transaction duration in state mode using time tags, or in timing mode
- Start- and stop-conditions and byte boundaries are detected by the analysis probe and displayed in timing mode
- View I<sup>2</sup>C symbolic address while in timing mode
- Operates simultaneously in both timing and state modes – no double-probing required
- Operates non-invasively in real-time at both 100 KHz and 400 KHz fast-mode
- Decodes 7-bit and 10-bit addresses in state mode
- Preprocessor display shows current message address and message count
- Save measurement setup time with predefined configuration software for the logic analyzer
- Does not require termination adapters
- Includes all of the features of the ALD-232 Analysis Probe (RS232, RS449, and IEEE1284)

### **1.3. Logic Analyzers Supported**

The I<sup>2</sup>C bus analysis probe may be used with all currently available 165XX and 167XX-system state analyzer modules, or with the 1660- or 1670-series logic analyzers. Two 17-channel pods are required.

### **1.4. Installing the Software**

The installation process is different depending upon the Agilent analyzer model. The disk contains the following files:

DISK1.DAT	MIXED.B
INDEX.TXT	STATE.B
INFO.TXT	I AAI 2C. I

#### **167xx Models:**

Insert the diskette included with this option into the 167xx floppy drive. Navigate to the *System Administrator Tools* tab of the analyzer. Select the *Software Install* tab. Next select the *Install...* feature. Under *Media*, choose *Flexible Disk* and then *Apply*. In the *Flexible Disk Packages* window, select the ALD-232-I2C package and click on *Install*. This will load both the data formatter and the configurations.

#### **165xx Models:**

On these older model analyzers, files are copied onto the analyzer's hard disk. From the diskette supplied, copy the files from the right column on the previous page [MIXED.B, STATE.B and IAAI2C.I] to an appropriate place on the 16500, 166x or 167x hard drive.

**Before installing the software onto your analyzer, we recommend that you make duplicate disks and store the original supplied diskette in a safe location in case of problems that may arise with your analyzer at a future point in time. If you do lose the original disk, these files may be downloaded from our website: [www.ald.com](http://www.ald.com).**

### **1.5. Equipment Supplied**

- RS232D, RS449, and IEEE 1284 and I<sup>2</sup>C Bus Analysis Probe
- This User Guide
- Diskette including configuration files and screen data formatter
- 2 flat ribbon 'Y' Cable for connecting to the target bus for RS232, RS449 and IEEE1284
- I<sup>2</sup>C attachment cable

### **1.6. Minimum Equipment Required**

In addition to the equipment supplied above, an Agilent or HP analyzer is required.

## 2. Installation

The ALD-232-I2C is easy to install. The unit is simply connected between the logic analyzer and the I<sup>2</sup>C target and the supplied configuration is loaded into the logic analyzer.

### 2.1. Initial Inspection

Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until the contents of the shipment have been inspected mechanically and electrically. If the contents are incomplete, if there is mechanical damage or defect, or if the instrument does not operate, notify Advanced Logical design, Inc.. If the shipping container is damaged, or the cushioning materials show signs of stress, notify the carrier as well as the ALD office. Keep the shipping materials for inspection by the carrier.

### 2.2. Connection to the Logic Analyzer

The ALD-232-I2C both derives its power from the logic analyzer and provides it data through the pod connection cables. Both pods 1 and 3 should be connected. Pod 1 provides state data and Pod 3 provides timing data. Note that Pod 2 is not used. The pod cables from the logic analyzer are plugged directly into the right side of the ALD-232. No additional terminators or adapters are required.

### 2.3. Connection to the Bus

The ALD-232-I2C has several connectors on the top of the unit that allow it to be attached to several busses. The connector used for the I<sup>2</sup>C bus is the one identified as J2. A short cable is supplied with a mating 26 pin IDC connector on one end and the other has 5 individual wires, terminated with sockets intended to connect to 0.025" square posts. These can be hooked directly to wirewrap posts on the unit under test or may be used with the grabbers supplied with the logic analyzer.

There are only 2 I<sup>2</sup>C signals, clock [SCL] and data [SDA]. These are connected to the unit under test from the supplied cable as shown in Table 1 below:

Cable Wire	Function
purple [0]	Ground
gray [1]	SCL
white [2]	Ground
black [3]	SDA
brown [4]	Ground
red [5]	NOT USED FOR I <sup>2</sup> C
orange [6]	NOT USED FOR I <sup>2</sup> C

**Table 1 – I<sup>2</sup>C cable signals**

## 2.4. Loading The Software

The software should be installed onto the logic analyzer as described in section 1.4. Loading the analyzer again differs between the 16500 and 16700 series analyzers.

### 16700 Analyzers

After the software has been installed, a new directory will be created on your analyzer:

```
/l o g i c / c o n f i g s / A L D / A L D 2 3 2 A _ I 2 C
```

In this directory will be 10 configuration files:

```
I 2 C _ S . _ _ A      I 2 C _ S . _ _ D      I 2 C _ S T . _ _ A      I 2 C _ S T . _ _ D
I 2 C _ S . _ _ B      I 2 C _ S . _ _ E      I 2 C _ S T . _ _ B      I 2 C _ S T . _ _ E
I 2 C _ S . _ _ C      I 2 C _ S T . _ _ C
```

The files that end with ST are State and Timing modes combined. The others files that end with S are State Only mode. The state only display will have an extra field (P3ADDR) that will show the captured I<sup>2</sup>C address. If you chose the state and timing configuration, that field will only be available in the timing display.

Load the configuration appropriate to the logic analyzer that you wish to use (16550, 16712, or 16717 respectively).

### 16500 Analyzers

From the directory that you copied the 16500 I2C files, you may load a state only display or a mixed state and timing display. If you use the state only display, you will have an extra field, P3ADDR, that shows the captured I<sup>2</sup>C address on each display line. If you choose the timing display, that field is available on the timing display only.

When loading either of these configurations, be sure to load only the slot that contains your logic analyzer. The default is to load ALL which will generate the message:

```
“ONE OR MORE CONFIGURATIONS NOT LOADED”
```

This means that the equipment loaded into your other slots have not been configured. The native logic analyzer for these configurations is the 16550. If you have another analyzer, the 16500 will attempt to convert the configuration for the installed analyzer.

The other file provided, IAAI2C.I is an ‘inverse assembler’ file and is used to format the state data in one of two ways. These two different formats are explained in section 4.4.

### 2.4.1. State Only Configuration

The State only configuration that is supplied sets up the logic analyzer pods 1 and 3 as follows in Table 2:

MASTER CLOCK: J1↑

NAME	POD 3 CHAN	POD 1 CHAN
DATA		8:1
FRAME		9
R/Wn		10
START		11
STOP		12
P3ADDR	9:0	
STAT		12:9, 0
/ACK		0
ADDR		0

**Table 2 – Pod set up for State Only Configuration**

### 2.4.2. Mixed Configuration

The Mixed configuration sets up Machine 1 as state and Machine 2 as timing. Machine 1 uses Pod 1 and Machine 2 uses Pod 3 as shown in Table 3 and Table 4. Since pods must be assigned as pairs, pods 2 and 4 may be used for other signals. Note that Machine 1, that has the spare Pod 2, must be clocked by the I<sup>2</sup>C analysis probe STROBE, and thus any of the user's signals on Pod 2 would be clocked with that STROBE as well.

#### Machine 1

MASTER CLOCK: J1↑

NAME	POD 1 CHAN
DATA	8:1
FRAME	9
R/Wn	10
START	11
STOP	12
P3ADDR	not assigned
STAT	12:9, 0
/ACK	0
ADDR	0

**Table 3 – Pod 1 Mixed Configuration**

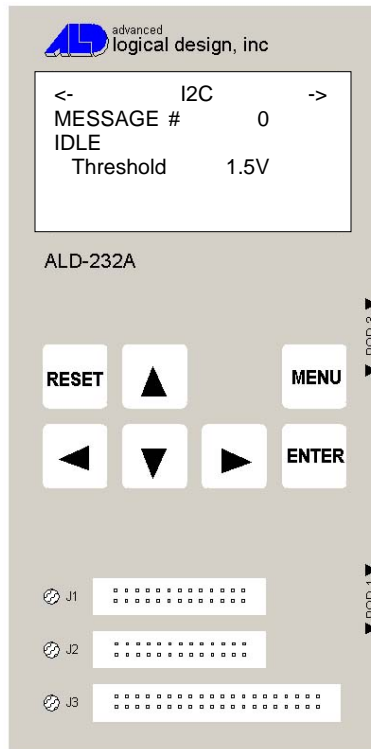
#### Machine 2

NAME	POD 3 CHAN
ADDRS	9:0
SCL	10
SDA	11
R/Wn	12
START	13
STOP	14
STROBE	Data on Clock L

**Table 4 – Pod 3 Mixed Configuration**

### 3. Operational Overview

Immediately after power is applied or **RESET** is depressed, the ALD-232-I2C will enter self-test mode. After the self-test is completed, the ALD-232-I2C will enter the RUN mode, with the interface connection (J1, J2 or J3) that was last used. [The first time the ALD-232-I2C is used, it will come up running in the I2C mode with interface levels set to TTL thresholds.] The LED opposite the appropriate connector (J2) will be lit. All operations of the ALD-232A are controlled by the keyboard (See Figure 1). When the logic analyzer cables are plugged into the ALD232A, the unit will power up in the mode it was last in. Navigation through the options is very simple. An arrow (->) will point to the item that can be changed. A new value may be selected for that item by scrolling through the choices with the ◀ and the ▶ keys. To move to a different item, use the ▲ and ▼ keys. The item at the top of the screen is the type of analysis desired [RS232 ASYNC, RS232 SYNC, RS449 ASYNC, RS449 SYNC, IEEE 1284 and I2C]. The last screen in the sequence is an informational screen.



**Figure 1: ALD-232-I2C top panel**

The operation of the ALD-232-I2C in modes other than I<sup>2</sup>C is explained in the basic ALD-232 manual, also enclosed. This addendum covers only the I<sup>2</sup>C operation.

## 4. Analyzing I<sup>2</sup>C

The I<sup>2</sup>C bus protocol has been adopted by many chip suppliers as an economical, simple solution to 8-bit digital control applications to avoid problems of confusion, data loss, and blockage of information, and to minimize the number of IC packages required to implement a circuit. The ALD-232-I2C conforms to the I<sup>2</sup>C specification as developed by Philips Semiconductor. It has been specifically designed to monitor data transfers, data validity, start and stop conditions, and data acknowledgement.

For an excellent tutorial and bus specification for the I<sup>2</sup>C bus, the reader is referred to:

80C51 Data Handbook, 1997 Edition, Philips Semiconductors.

### 4.1. Setting Threshold Voltage

The ALD-232-I2C provides for an adjustable voltage threshold for SCL and SDA. This permits its use in systems that use other than TTL voltages. The switching (threshold) voltage may be set from 0.5v to 3.0v. The default value is 1.5v.

To set the threshold voltage go to the I<sup>2</sup>C option screen (See Figure 2), press the ▼ on the ALD-232-I2C. This will move the selection arrow down to the threshold voltage line. Use the ◀ and the ▶ until the desired voltage appears [in the range of 0.5v to 3.0v]. The selection will be saved for the next power up if either 5 seconds pass or if the **enter** key is depressed.

```
          I2C
MESSAGE #      0
IDLE
->Threshold    1.5V
```

Figure 2 – Setting the threshold voltage

### 4.2. Run Time Display

When the analysis probe is running an I<sup>2</sup>C measurement, the unit's display will show the following information (See Figure 3):

```
          I2C
MESSAGE #      nnnnn
WRITING aaa
->Threshold    1.5V
```

Figure 3 – I<sup>2</sup>C display during run

The second display line will denote the number of frames received. The MESSAGE # will show the counts (nnnnn) from 0 to 65536. The third display line shows the most

recent frame's address (aaa) and if it was READ or WRITE transfer. On the fourth line the 1.5V on the display line indicates the threshold voltage that was set (or default if not explicitly set).

### 4.3. Logic Analyzer Connections

The ALD-232-I2C supports simultaneous state and timing analysis. POD 1 is used for state analysis and POD 3 is for timing. For state analysis, the analysis probe accumulates the serial data and presents it to the logic analyzer as bytes along with some control signals on POD 1. The signals on POD 3 are buffered versions of SDA and SCL, the same control signals from POD 1 repeated and a 10-bit address is provided by the analysis probe after decoding the address byte(s).

The organization of these signals is shown in Tables 5 and 6 below.

POD 1 channel	Signal
8:0	Data Byte + ACK bit
9	FRAME
10	Read/Write*
11	START
12	STOP
clk	podClk

**Table 5 – Pod 1 signals**

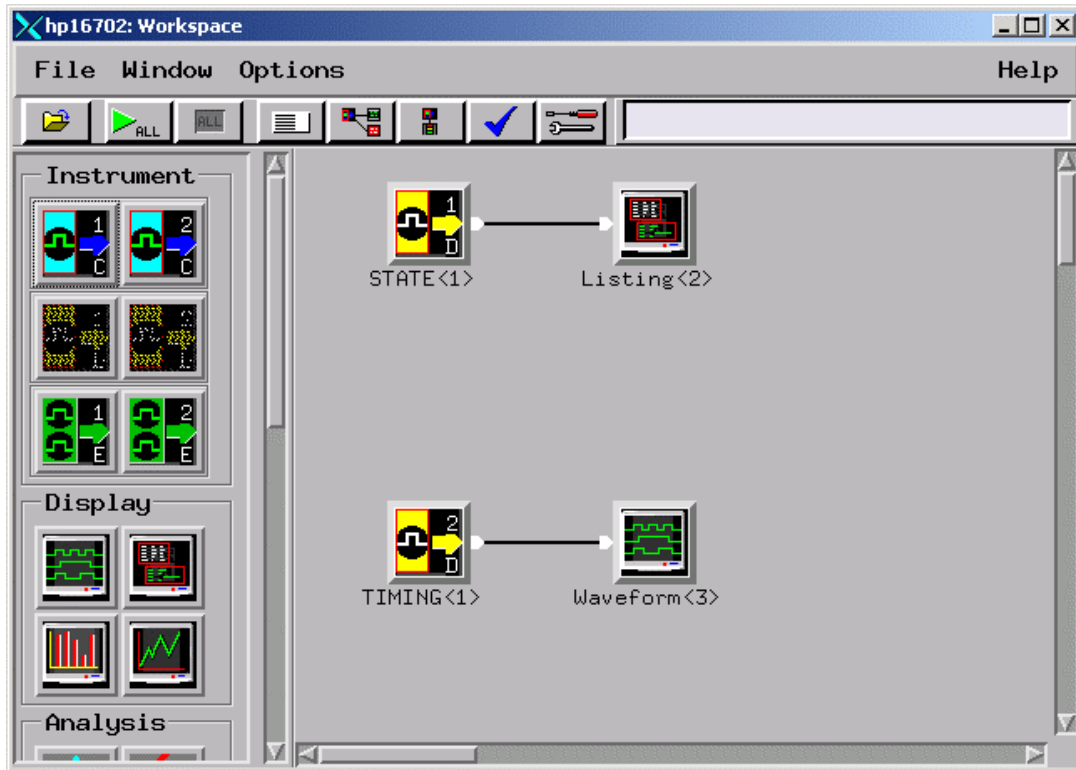
POD 3 channel	Signal
9:0	Address
10	SCL I <sup>2</sup> C clock
11	SDA I <sup>2</sup> C data
12	Read/Write*
13	START
14	STOP
clk	podClk

**Table 6 – Pod 3 signals**

### 4.4. State Analysis

#### 4.4.1. Choosing Logic Analyzer Display

The configuration files supplied with the ALD-232-I2C option for the 16700 series logic analyzers include both a state and timing or state only analysis. The workspace for state and timing is shown below (See Figure 4):

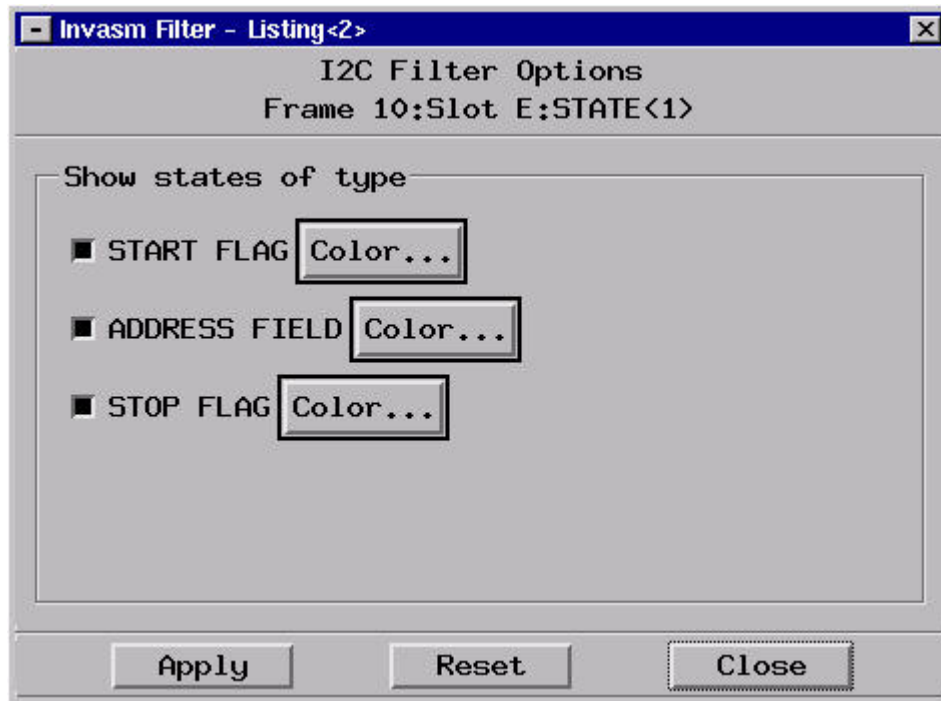


**Figure 4 – Workspace setup for I<sup>2</sup>C configurations**

The ‘as shipped’ configuration for the trigger has the timing analyzer slaved to trigger after the state analyzer. The user may create any triggering situation appropriate to the problem being solved.

Both 16500 and 16700 users have 2 configurations to choose from, a state only and a mixed configuration. In the state only configuration, an additional field, P3ADDR, is available that contains the last value from the I<sup>2</sup>C address byte(s). In the mixed configuration, both state and timing are available. The P3ADDR field will only be available to the timing display.

The user has a choice of two different types of state display (on both the 16700 and 16500). The difference is the amount of detail. In the low level display format, each line of the display is annotated showing the contents of that byte or flag. In the 16700, START flags, STOP flags and ADDRESS bytes are given different colors. The user may change these colors or even choose not to display some of these field types. This is accomplished through the INVASM>FILTER menu option. That choice is shown below (See Figure 5):



**Figure 5 – I<sup>2</sup>C filter options**

This option is not available on the 16500.

An example of a low-level display format is shown below (See Figure 6):

State Number	ALD	Time	DATA	FRAME	R/Wn	START	STOP
Decimal	I2C Formatter	Absolute	Hex	Binary	Binary	Binary	Binary
11	STOP	2,590 ms	18	0	0	0	1
12	START	2,848 ms	18	1	0	1	0
13	ADDRESS 7Fh	2,948 ms	7F	1	0	0	0
14	Read FFh NAK	3,485 ms	FF	1	1	0	0
15	STOP	3,671 ms	FF	0	1	0	1
16	START	4,021 ms	FF	1	1	1	0
17	ADDRESS 4Dh	4,120 ms	4D	1	1	0	0
18	Read FFh	4,460 ms	FF	1	1	0	0
19	Read FFh	4,687 ms	FF	1	1	0	0
20	Read FFh	4,921 ms	FF	1	1	0	0
21	Read FFh NAK	5,337 ms	FF	1	1	0	0
22	STOP	5,522 ms	FF	0	1	0	1
23	START	6,006 ms	FF	1	1	1	0
24	ADDRESS 9Eh	6,106 ms	9E	1	1	0	0
25	Write 40h	6,364 ms	40	1	0	0	0
26	Write 53h	6,581 ms	53	1	0	0	0
27	STOP	6,795 ms	A6	0	0	0	1
28	START	7,095 ms	A6	1	0	1	0
29	ADDRESS A2h	7,194 ms	A2	1	0	0	0
30	Write 02h	7,452 ms	02	1	0	0	0
31	START	7,798 ms	04	1	0	1	0
32	ADDRESS A3h	7,898 ms	A3	1	0	0	0
33	Read 28h NAK	8,352 ms	28	1	1	0	0
34	STOP	8,537 ms	51	0	1	0	1
35	START	10,261 ms	51	1	1	1	0
36	ADDRESS 74h	10,361 ms	74	1	1	0	0
37	Write 00h	10,619 ms	00	1	0	0	0
38	Write FDh	10,837 ms	FD	1	0	0	0
39	Write FCh	11,054 ms	FC	1	0	0	0
40	Write FCh	11,272 ms	FC	1	0	0	0
41	Write F6h	11,490 ms	F6	1	0	0	0
42	STOP	11,703 ms	EC	0	0	0	1
43	START	12,824 ms	EC	1	0	1	0
44	ADDRESS 76h	12,924 ms	76	1	0	0	0
45	Write 01h	13,182 ms	01	1	0	0	0
46	Write 02h	13,400 ms	02	1	0	0	0
47	Write 3Eh	13,617 ms	3E	1	0	0	0
48	Write 7Fh	13,835 ms	7F	1	0	0	0

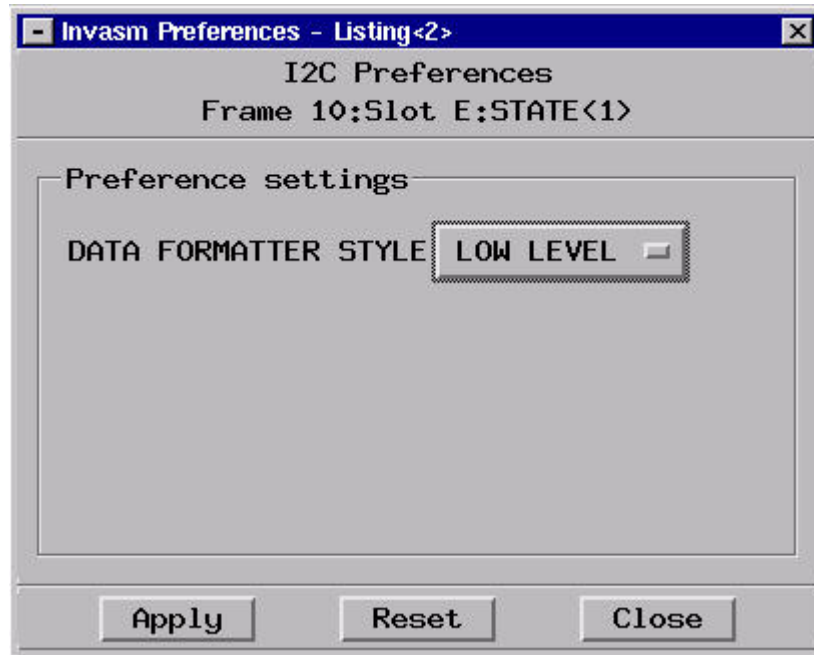
Figure 6 – State ‘low level’ display

The user may opt for a higher level of interpretation where the I<sup>2</sup>C message is displayed horizontally on one (or more) lines. This is shown below (See Figure 7):

State Number	ALD	Time	DATA	FRAME	R/Wn	START	STOP
Decimal	I2C Formatter	Absolute	Hex	Binary	Binary	Binary	Binary
11		2,590 ms	18	0	0	0	1
12		2,848 ms	18	1	0	1	0
13		2,948 ms	7F	1	0	0	0
14	@ 7Fh Read FF	3,485 ms	FF	1	1	0	0
15		3,671 ms	FF	0	1	0	1
16		4,021 ms	FF	1	1	1	0
17		4,120 ms	4D	1	1	0	0
18	@ 4Dh Read FF FF FF FF	4,460 ms	FF	1	1	0	0
19		4,687 ms	FF	1	1	0	0
20		4,921 ms	FF	1	1	0	0
21		5,337 ms	FF	1	1	0	0
22		5,522 ms	FF	0	1	0	1
23		6,006 ms	FF	1	1	1	0
24		6,106 ms	9E	1	1	0	0
25	@ 9Eh Wrote 40 53	6,364 ms	40	1	0	0	0
26		6,581 ms	53	1	0	0	0
27		6,795 ms	A6	0	0	0	1
28		7,095 ms	A6	1	0	1	0
29		7,194 ms	A2	1	0	0	0
30	@ A2h Wrote 02	7,452 ms	02	1	0	0	0
31		7,798 ms	04	1	0	1	0
32		7,898 ms	A3	1	0	0	0
33	@ A3h Read 28	8,352 ms	28	1	1	0	0
34		8,537 ms	51	0	1	0	1
35		10,261 ms	51	1	1	1	0
36		10,361 ms	74	1	1	0	0
37	@ 74h Wrote 00 FD FC FC	10,619 ms	00	1	0	0	0
38		10,837 ms	FD	1	0	0	0
39		11,054 ms	FC	1	0	0	0
40		11,272 ms	FC	1	0	0	0
41		11,490 ms	F6	1	0	0	0
42		11,703 ms	EC	0	0	0	1
43		12,824 ms	EC	1	0	1	0
44		12,924 ms	76	1	0	0	0
45	@ 76h Wrote 01 02 3E 7F	13,182 ms	01	1	0	0	0
46		13,400 ms	02	1	0	0	0
47		13,617 ms	3E	1	0	0	0
48		13,835 ms	7F	1	0	0	0

Figure 7 – State ‘high level’ display

To choose between these 2 formats, the user selects the INVASM menu item. In the 16700, select INVASM>PREFERENCES and the dialog box below will appear (See Figure 8):



**Figure 8 – Inverse Assembler Preferences**

Click on the box to select either LOW LEVEL or HIGH LEVEL and then APPLY. 16500 users will see that option when they select the INVASM box at the top of the display.

#### 4.4.2. Interpreting the Display

The two displays above include several fields. The central field, DATA, is interpreted by the 'inverse assembler'. If the DATA field is shown in some other format (HEX, DECIMAL, etc.) on your display, select the format bar under the field DATA and the drop down menu will allow INVASM to be selected. The two different display formats contain the same data, one presents vertically and the other horizontally.

The Low Level vertical display shown below presents one line for each event or byte detected on the I<sup>2</sup>C bus (See Figure 9). In the example, line twelve shows the detected start event. After START, the protocol requires either a 7 or 10 bit address, which is shown next. A READ of FFh follows, which was not acknowledged, and then a STOP occurs to flag the end of the READ event.

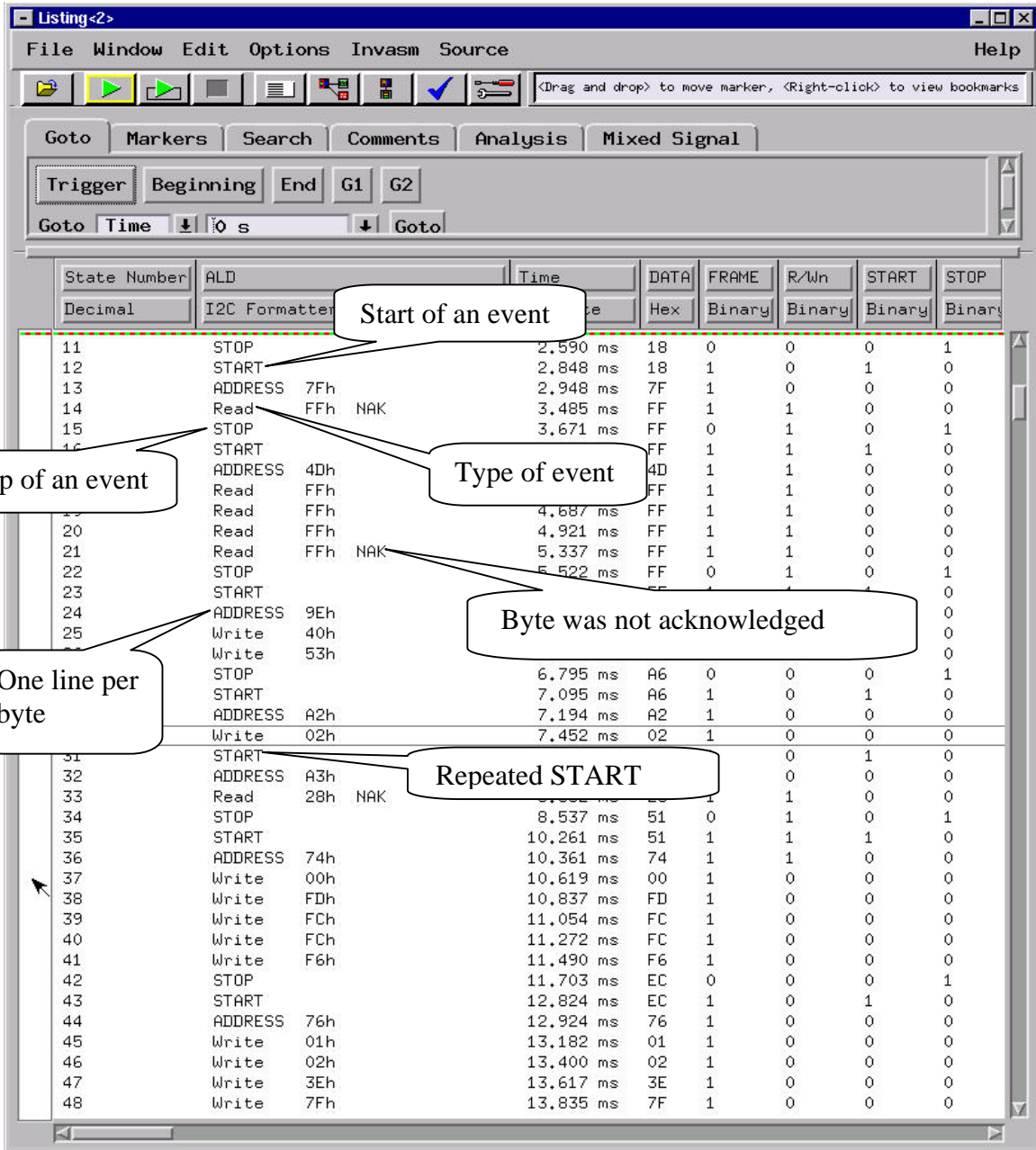


Figure 9 – Description of State ‘low level’ display

Addresses displayed are either 7 bit or 10 bit addresses, depending upon which I<sup>2</sup>C format. The 7 bit address is displayed as an 8 bit quantity with the LSB=0. This seems to be customary with I<sup>2</sup>C. For example, the first byte received after the start condition is:

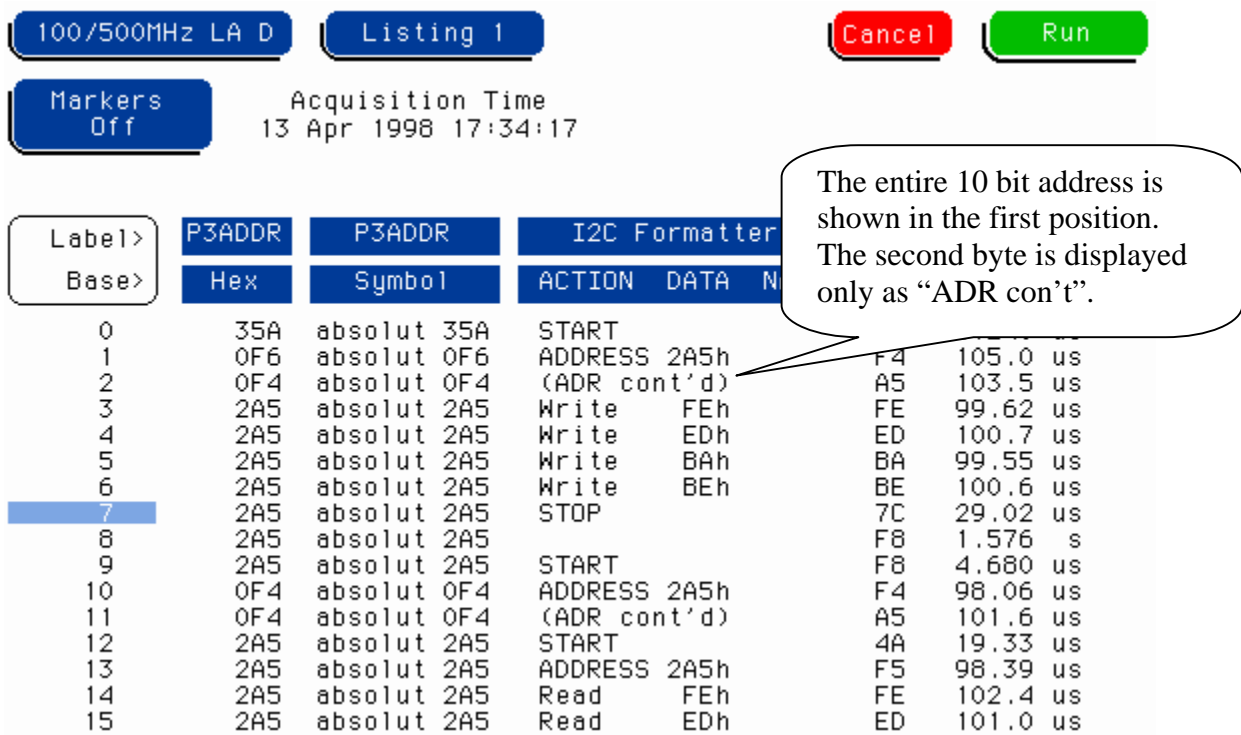
11111111

This would be displayed as address 7F, even though it is a ‘7 bit’ address. The LSB is actually the R/W control. In the case where the frame is a write operation, the same address would be:

11111110

but this would also be displayed as 7F since the R/W control is masked for the purpose of the display on the logic analyzer.

Ten bit addresses utilize 2 bytes in the I<sup>2</sup>C format. To distinguish 10 bit addresses from 7 bit addresses, the first byte in the protocol uses a special encoding to identify the address as 10 bit [1111 0aaR]. The upper 2 bits of the 10 bit address are aa and the R/W bit is R, as usual. The following byte contains the remaining 8 bits of the address. The display for a bit address is shown below (See Figure 10):



**Figure 10 – Handling of 10-bit address**

The length of an I<sup>2</sup>C frame is not specified and can continue as long as the master wishes to continue and the slave does not terminate it. Each byte transferred is required to be acknowledged by the receiving party (either master or slave). If the receiver does not acknowledge, the master will abort the transfer.

In both versions of the display, when a data byte is acknowledged, nothing is shown on the display line. However, if the receiver fails to acknowledge a byte, the symbol NAK will be shown. In the example above, note that the next event was transfer abort (STOP) presented by the master (See Figure 9).

The High Level presentation shown below does not explicitly show the start and stop events (See Figure 11), but only displays the data transferred and the address. In the example, the first transfer is a single byte read from address 7Fh. The '@' symbol shown in the display is an implicit indicator of a start event since the address always follows the start.

If the transfer length exceeded 4 bytes, only the data bytes would be shown on successive lines. The reason for the large amount of 'white' space between lines is due to the logic analyzer's clocking. Every byte captured by the logic analyzer must be displayed on a separate line. This maintains display synchronization with the other fields that may be displayed.

Listing<2>

File Window Edit Options Invasm Source Help

Goto Markers Search Comments Analysis Mixed Signal

Trigger Beginning End G1 G2

Goto Time ↓ 0 s ↓ Goto

State Number	ALD	Time	DATA	FRAME	R/Wn	START	STOP
Decimal	I2C Formatter	Absolute	Hex	Binary	Binary	Binary	Binary
11		2.590 ms	18	0	0	0	1
12		2.848 ms	18	1	0	1	0
13		2.948 ms	7F	1	0	0	0
14	@ 7Fh Read FF	3.485 ms	FF	1	1	0	0
15		3.671 ms	FF	0	1	0	1
		4.021 ms	FF	1	1	1	0
		4.120 ms	4D	1	1	0	0
	@ 4Dh Read FF FF FF FF	4.460 ms	FF	1	1	0	0
20					1	0	0
21					1	0	0
22					1	0	1
23					1	1	0
24					1	0	0
25	@ 9Eh Wrote 40 53				0	0	0
26		6.581 ms	53	1	0	0	0
27		6.795 ms	A6	0	0	0	1
28		7.095 ms	A6	1	0	1	0
29		7.194 ms	A2	1	0	0	0
30	@ A2h Wrote 02	7.452 ms	02	1	0	0	0
31		7.798 ms	04	1	0	1	0
32		7.898 ms	A3	1	0	0	0
33	@ A3h Read 28	8.352 ms	28	1	1	0	0
34		8.537 ms	51	0	1	0	1
35		10.261 ms	51	1	1	1	0
36		10.361 ms	74	1	1	0	0
37	@ 74h Wrote 00 FD FC FC	10.619 ms	00	1	0	0	0
38		10.837 ms	FD	1	0	0	0
39		11.054 ms	FC	1	0	0	0
40					0	0	0
41					0	0	0
42					0	1	1
43					1	1	0
44					0	0	0
45	@ 76h Wrote 01 02 3E 7F	13.182 ms	01	1	0	0	0
46		13.400 ms	02	1	0	0	0
47		13.617 ms	3E	1	0	0	0
48		13.835 ms	7F	1	0	0	0

Denotes START

Several bytes together

Due to exceeding 4 bytes in transfer

Figure 11 – Description of State ‘high level’ display

The fields in the default display for the State Only Configuration are shown in Figure 12:

P3ADDR	P3ADDR	ALD	Time	DATA	FRAME
Hex	Symbols	I2C Formatter	Absolute	Hex	Binary

**Figure 12 – Fields for State Only configuration**

The only field processed by the ‘inverse assembler’ or formatter is the "ALD" field above. The others are just the data as it appears when the I<sup>2</sup>C data byte is completed. The P3ADDR is the current I<sup>2</sup>C address captured by the analysis probe. Note that the P3 in P3ADDR indicates that it comes from Pod 3 and would not be available on the state display if simultaneous state and timing were displayed since Pod 3 is the timing pod.

The example above illustrates the use of multiple displays of the same field, in this case, P3ADDR. The first column displays the I<sup>2</sup>C address as a hex value while the second column displays it as a symbol (See Figure 12).

The logic analyzer provides the capability of displaying a field in various numeric formats and a symbol format. Since each I<sup>2</sup>C address represents a physical device, it may be convenient to present the name of that device instead of its numeric address. To accomplish this, set up a symbol table in the FORMAT menu. An example symbol table (See Figure 13) and its resulting output (See Figure 14) is illustrated below:

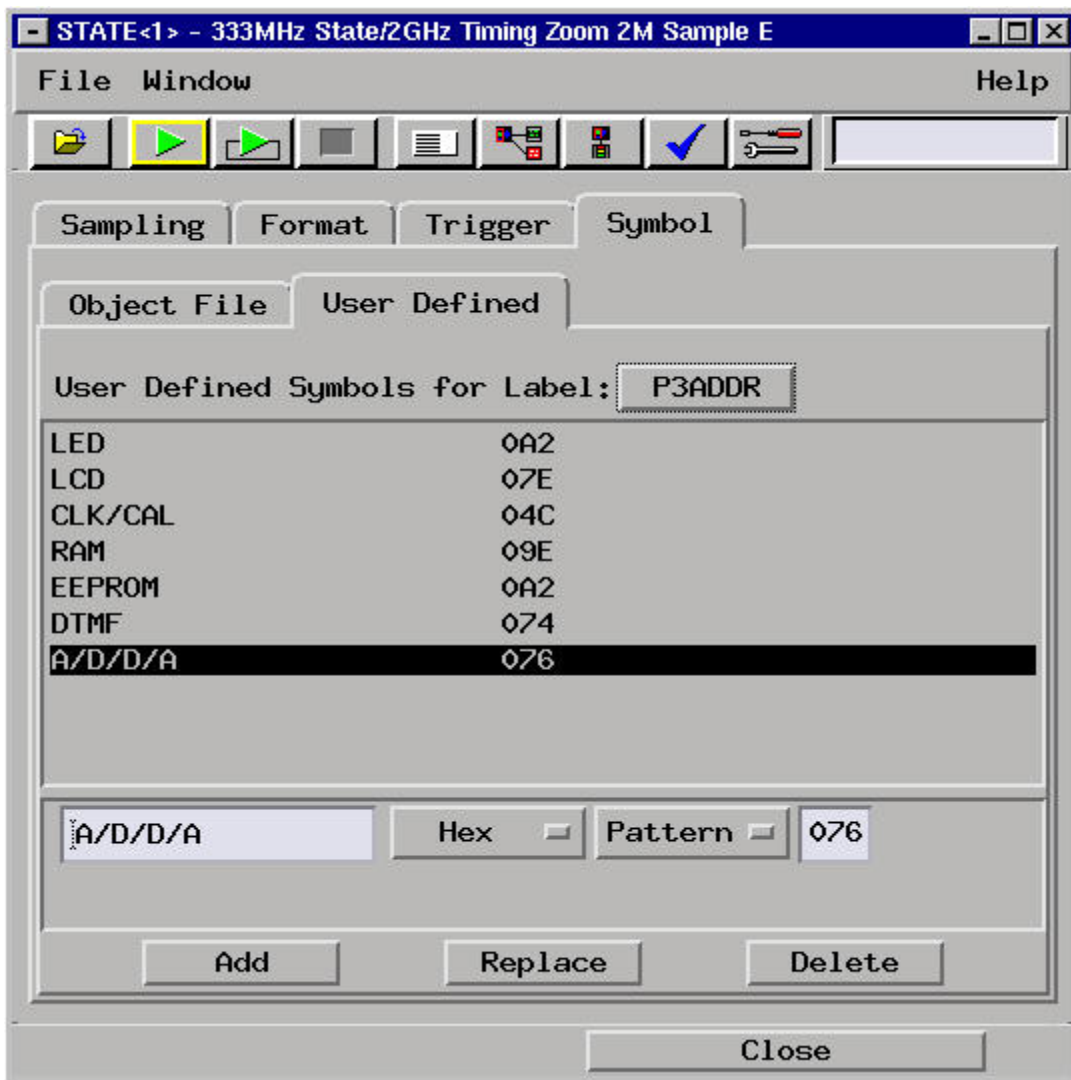


Figure 13 – User defined symbols

State Number	P3ADDR	P3ADDR	ALD	Time	DATA	FRAME	R
Decimal	Hex	Symbols	I2C Formatter	Absolute	Hex	Binary	B
0	0A2	LED	START	0 s	0A	1	0
1	0A2	LED	ADDRESS A2h	99.780 us	A2	1	0
2	0A2	LED	Write 00h	357.772 us	00	1	0
3	0A2	LED	START	703.612 us	00	1	0
4	0A2	LED	ADDRESS A3h	803.392 us	A3	1	0
5	0A2	LED	Read 0Dh NAK	1.257 ms	0D	1	1
6	0A2	LED	STOP	1.443 ms	1B	0	1
7	0A2	LED	START	1.801 ms	1B	1	1
8	0A2	LED	ADDRESS A2h	1.901 ms	A2	1	1
9	0A2	LED	Write 00h	2.159 ms	00	1	0
10	0A2	LED	Write 0Ch	2.376 ms	0C	1	0
11	0A2	LED	STOP	2.590 ms	18	0	0
12	0A2	LED	START	2.848 ms	18	1	0
13	0A2	LED	ADDRESS 7Fh	2.948 ms	7F	1	0
14	07E	LCD	Read FFh NAK	3.485 ms	FF	1	1
15	07E	LCD	STOP	3.671 ms	FF	0	1
16	07E	LCD	START	4.021 ms	FF	1	1
17	07E	LCD	ADDRESS 4Dh	4.120 ms	4D	1	1
18	04C	CLK/CAL	Read FFh	4.460 ms	FF	1	1
19	04C	CLK/CAL	Read FFh	4.687 ms	FF	1	1
20	04C	CLK/CAL	Read FFh	4.921 ms	FF	1	1
21	04C	CLK/CAL	Read FFh NAK	5.337 ms	FF	1	1
22	04C	CLK/CAL	STOP	5.522 ms	FF	0	1
23	04C	CLK/CAL	START	6.006 ms	FF	1	1
24	04C	CLK/CAL	ADDRESS 9Eh	6.106 ms	9E	1	1
25	09E	RAM	Write 40h	6.364 ms	40	1	0
26	09E	RAM	Write EDh	6.581 ms	ED	1	0
27	09E	RAM	STOP	6.795 ms	DA	0	0
28	09E	RAM	START	7.095 ms	DA	1	0
29	09E	RAM	ADDRESS A2h	7.194 ms	A2	1	0
30	0A2	LED	Write 02h	7.452 ms	02	1	0
31	0A2	LED	START	7.798 ms	04	1	0
32	0A2	LED	ADDRESS A3h	7.898 ms	A3	1	0
33	0A2	LED	Read 03h NAK	8.352 ms	03	1	1

**Figure 14 – Display with user-defined symbols**

The other DATA field is the raw byte data (without the ACK bit) from the analysis probe. This is included in the state display to allow other than hex data presentations. The format field can be used to select any available format [e.g. ASCII, BINARY, OCTAL, ...etc].

The TIME field is generated by the logic analyzer and shows the arrival time of each data byte, either in absolute or relative time.

## 4.5. Timing Analysis

SDA and SCL are presented to the logic analyzer on Pod 3 and may be used to view the signal timing either separately or in conjunction with the state display. In addition to the two basic bus signals, the analysis probe also provides some additional signals that assist the timing display (See Figure 15).

The analysis probe will capture the I<sup>2</sup>C address after detecting the start event and will provide this as a 10-bit field that can be displayed with the timing. Note that this field cannot be accurate until after the 1<sup>st</sup> or 2<sup>nd</sup> byte of the frame (depending upon the address mode). In addition to the address, the type of transfer, read or write, is also provided for the timing display, but with the same validity restriction

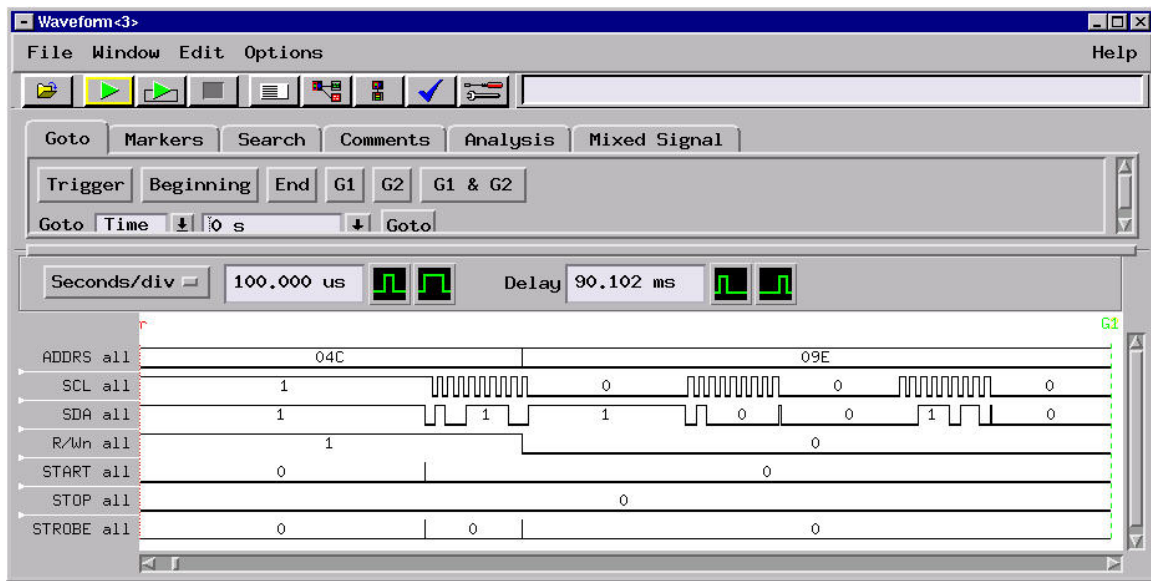


Figure 15 – Timing display

In addition, separate pulses are generated by the analysis probe identifying the start and stop events and at each byte boundary to assist in timing interpretation. The screen shot on the next page illustrates some of the timing features (See Figure 16). Note that STROBE occurs for every event, i.e. START, STOP and byte boundary.

SCL and SDA displayed in timing mode have been delayed from the probed inputs. This happens as a result of passing through the adjustable input comparator and a buffer. This is not serious since the skew between SDA and SCL is, worst case, less than 10 ns and this is far less than the specified rise and fall times (300 ns.). The only time one should keep this in mind is when probing other signals in conjunction with the I<sup>2</sup>C bus.

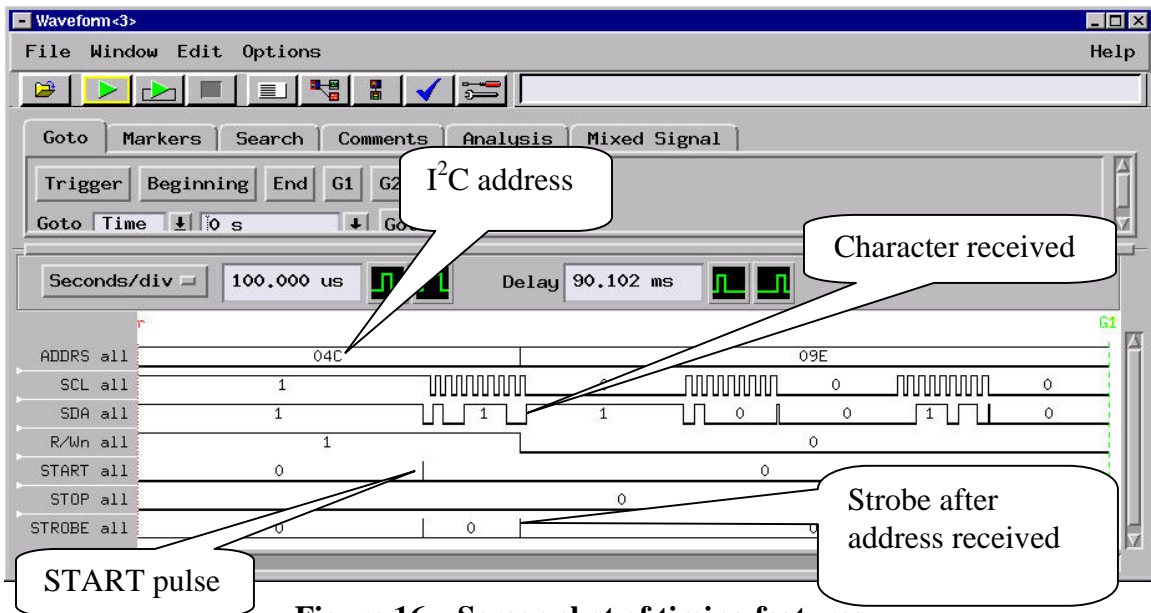
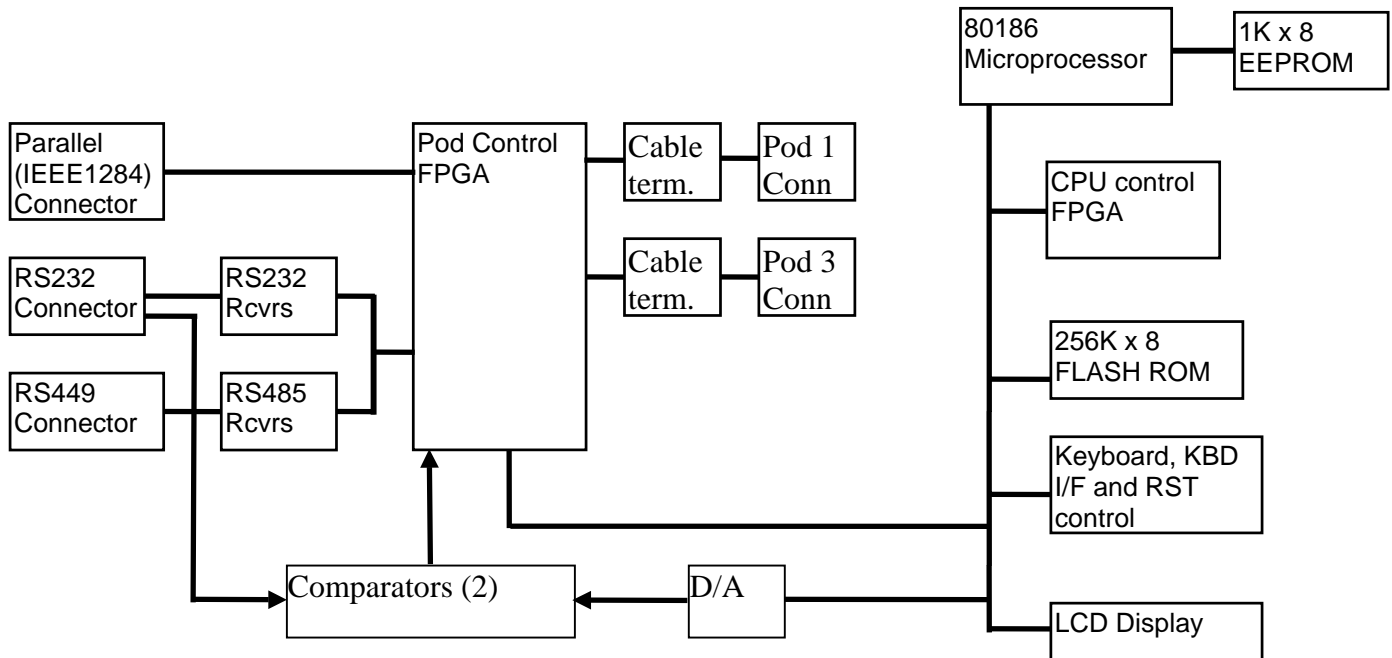


Figure 16 – Screen shot of timing features

## 5. Theory of Operation

The block diagram of the ALD-232-I2C analysis probe is shown below (See Figure 17):



**Figure 17 – Diagram of operation**

The ALD-232-I2C is a complete small processor system, with RAM, ROM, keyboard and display and a data capture system. The microprocessor system downloads the FPGAs with code appropriate to the operation selected, and receives parametric data from the user to program both FPGAs

The 80186-microprocessor system is conventional in design with the processor running at 32 MHz. Each time that the user selects a new parameter or option, that selection is recorded in the EEPROM. Data is also stored in the EEPROM after any mode change persists for more than 5 secs. This allows that selection to survive power loss. The Flash PROM contains not only the operational code, but also binary images of the code in both FPGAs. The CPU Control FPGA is downloaded automatically from the FPROP prior to the release of RESET from the 186. The Pod Control FPGA is downloaded under program control with code for RS232, RS449, IEEE1284 or I<sup>2</sup>C or any option that may be included.

The Pod Control FPGA collects data from the appropriate interface, RS232, RS449, IEEE1284 or and presents it to the pins of the logic analyzer. The FPGA acts as a dual UART or USRT for serial modes and an I<sup>2</sup>C receiver for that bus.

In I<sup>2</sup>C mode, the SDA and SCL inputs are connected via the RS232 (J2) port to 2 comparators, whose reference voltage has been set from a D/A converter on the uP bus. This is the user selectable threshold voltage. After level detection, they are sent to the Pod Control FPGA. This FPGA contains all of the necessary logic to process the I<sup>2</sup>C signals, START and STOP detection, address detection, serial to parallel converter, etc.

The FPGA directly generates the signals that are sent to the logic analyzer's Pod 1 and Pod 3.

Rev B

Advanced Logical Design, Inc.  
12280 Saratoga-Sunnyvale Road. Suite 201  
Saratoga, CA 95070  
Voice: (408)446-1004  
Fax: (408)446-1079  
email: [techsup@ald.com](mailto:techsup@ald.com)  
URL: <http://www.ald.com>