

USER GUIDE
I²C OPTION
FOR THE ALD-232A
BUS ANALYSIS PROBE
(Supplement for the Agilent 1680/90)



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1. Introduction

The I²C option for the ALD-232A-I2C analysis probe allows users to examine the operation of an I²C bus without having to manually decipher the serial protocol for the bus. The ALD-232A-I2C analysis probe will display the data on the bus in an easy to read byte format.

1.1. Specifications

- Bus Loading: 20kΩ shunted by 30 pF (at probe tip)
- Probe Cable length: 15 in
- Connectors: female 0.025" square post
- Power Required: ~ 325 mA supplied by the logic analyzer
- Mechanical: 4.0" x 7.5" x 2.0"
- Signals supported: SDA and SCL.
- Skew: skew due to signal buffering less than 10ns
- Max Delay (SCL,SDA): 22 ns
- Bus Speed: Both 100 KHz. and 400 KHz. speeds

1.2. Features

- I²C bus serial information is displayed as parallel bytes in state mode
- Flexible display modes provide detail or overview of bus transactions
- Quickly determine the information content of I²C transactions
- Operates at low voltage with user-defined threshold levels of 0.5V to 3.0V
- View details of I²C bus timing with signal pass-through mode
- View transaction duration in state mode using time tags, or in timing mode
- Start- and stop-conditions and byte boundaries are detected by the analysis probe and displayed in timing mode
- View I²C symbolic address while in timing mode
- Operates non-invasively in real-time at both 100 KHz and 400 KHz fast-mode
- Decodes 7-bit and 10-bit addresses in state mode
- Preprocessor display shows current message address and message count
- Save measurement setup time with predefined configuration software for the logic analyzer
- Does not require termination adapters
- Includes all of the features of the ALD-232A Analysis Probe (RS232, RS449, and IEEE1284)

1.3. Logic Analyzers Supported

The I²C bus analysis probe may be used with all currently available 165XX and 167XX-system state analyzer modules, or with the 1660-, 1670-, and 1680/90- series logic analyzers. Two 17-channel pods are required. This manual only discusses operation with the 1680/90/900 series analyzers. See the other manual included for operation with the 16700 family.

1.4. Installing the Software

A CDROM is supplied with the I²C option for 1680/90/900 analyzers. Insert the CD into the drive in the analyzer. Click on the **START** menu and select **RUN**. When the **RUN** dialog box appears, browse to **Installation_Files\I2C\setup.exe** on the CD. This will start the installation process. Click **NEXT** on each screen until the final screen, then click **FINISH**.

NOTE: Revision 3.x or later must be installed from Agilent before opening the configurations

This will install the data formatter program used for displaying the data from the I²C pod. It will also install 9 configuration files in a directory structure it creates:

C:\Documents and Settings*current_user*\My Documents\Agilent Technologies\Logic Analyzer\Config Files\I2C

state.xml	This configuration provides the most compact I ² C data display
state_DATA.xml	I ² C configuration with DATA
state_DATA01of01.mfb	I ² C DATA file
state_filtered.xml	This configuration displays each data packet on a single line
state_filtered_DATA.xml	I ² C configuration with DATA
state_filtered_DATA01of01.mfb	I ² C DATA file
timing.xml	This configuration displays the I ² C signals
timing_DATA.xml	I ² C configuration with DATA
timing_DATA01of01.mfb	I ² C DATA file

Note: .xml Configurations with “DATA” in the title contain captured data and can be used for demonstration purposes. They must be viewed “OFFLINE”.

1.5. Equipment Supplied

- RS232D, RS449, and IEEE 1284 and I²C Bus Analysis Probe
- This User Guide
- A User Guide for the 16700 series analyzer
- Diskette including configuration files and screen data formatter for the 16700 family

- CDROM with configuration and data formatter files for the 1680/90/900
- 2 flat ribbon 'Y' Cable for connecting to the target bus for RS232, RS449 and IEEE1284
- I²C attachment cable

1.6. Minimum Equipment Required

In addition to the equipment supplied above, an Agilent 1680, 1690 or 16900 logic analyzer is required.

2. Installation

The ALD-232A-I2C is easy to install. The unit is simply connected between the logic analyzer and the I²C target and the supplied configuration is loaded into the logic analyzer.

2.1. Initial Inspection

Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until the contents of the shipment have been inspected mechanically and electrically. If the contents are incomplete, if there is mechanical damage or defect, or if the instrument does not operate, notify Advanced Logical design, Inc. If the shipping container is damaged, or the cushioning materials show signs of stress, notify the carrier as well as the ALD office. Keep the shipping materials for inspection by the carrier.

2.2. Connection to the Logic Analyzer

The ALD-232A-I2C both derives its power from the logic analyzer and provides it data through the pod connection cables. Both pods 1 and 3 should be connected. Pod 1 provides state data and Pod 3 provides timing data. Note that Pod 2 is not used. The pod cables from the logic analyzer are plugged directly into the right side of the ALD-232A. No additional terminators or adapters are required.

2.3. Connection to the Bus

The ALD-232A-I2C has several connectors on the top of the unit that allow it to be attached to several busses. The connector used for the I²C bus is the one identified as J2. A short cable is supplied with a mating 26 pin IDC connector on one end and the other has 5 individual wires, terminated with sockets intended to connect to 0.025" square posts. These can be hooked directly to wirewrap posts on the unit under test or may be used with the grabbers supplied with the logic analyzer.

There are only 2 I²C signals, clock [SCL] and data [SDA]. These are connected to the unit under test from the supplied cable as shown in Table 1 below:

Cable Wire	Function
purple [0]	Ground
gray [1]	SCL
white [2]	Ground
black [3]	SDA
brown [4]	Ground
red [5]	NOT USED FOR I ² C
orange [6]	NOT USED FOR I ² C

Table 1 – I²C cable signals

2.4. Loading The Configurations

There are three supplied configurations with the 1680 version of the I²C.

1. A detailed state analysis display,
2. A filtered state analysis display and
3. A timing display.

The configurations can be found at: C:\Documents and Settings\current_user\My Documents\Agilent Technologies\Logic Analyzer\Config Files\I2C

2.4.1. Both State Configurations

Load **state.xml** from the file menu of the logic analyzer. It will configure the analyzer for state analysis with the clock source as POD 1 rising clock as shown in Figure 1.

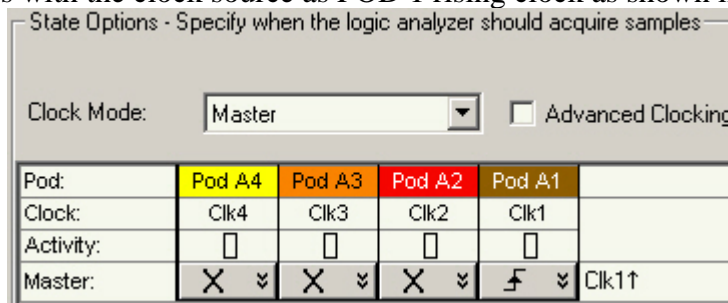


Figure 1: State Clock Configuration

It will also configure the pod channels as shown in Figure 2. Note that POD 2 is unused. That is for backwards compatibility with the 16700 family and may be changed if the user desires.

3. Operational Overview

Immediately after power is applied or **RESET** is depressed, the ALD-232A-I2C will enter self-test mode. After the self-test is completed, the ALD-232A-I2C will enter the RUN mode, with the interface connection (J1, J2 or J3) that was last used. [The first time the ALD-232A-I2C is used, it will come up running in the I²C mode with interface levels set to TTL thresholds.] The LED opposite the appropriate connector (J2) will be lit.

All operations of the ALD-232A are controlled by the keyboard (See Figure 4). When the logic analyzer cables are plugged into the ALD-232A, the unit will power up in the mode it was last in. Navigation through the options is very simple. An arrow (→) will point to the item that can be changed. A new value may be selected for that item by scrolling through the choices with the ◀ and the ▶ keys. To move to a different item, use the ▲ and ▼ keys. The item at the top of the screen is the type of analysis desired [RS232 ASYNC, RS232 SYNC, RS449 ASYNC, RS449 SYNC, IEEE 1284 and I2C]. The last screen in the sequence is an informational screen.

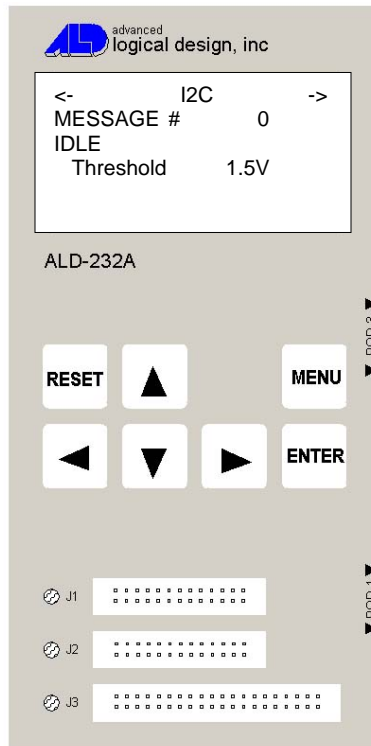


Figure 4: ALD-232A-I2C top panel

The operation of the ALD-232-I2C in modes other than I²C is explained in the basic ALD-232 manual, also enclosed. This addendum covers only the I²C operation.

4. Analyzing I²C

The I²C bus protocol has been adopted by many chip suppliers as an economical, simple solution to 8-bit digital control applications to avoid problems of confusion, data loss, and blockage of information, and to minimize the number of IC packages required to implement a circuit. The ALD-232A-I2C conforms to the I²C specification as developed by Philips Semiconductor. It has been specifically designed to monitor data transfers, data validity, start and stop conditions, and data acknowledgement.

For an excellent tutorial and bus specification for the I²C bus, the reader is referred to:

80C51 Data Handbook, 1997 Edition, Philips Semiconductors. Philips also publishes the specification separately.

4.1. Setting Threshold Voltage

The ALD-232A-I2C provides for an adjustable voltage threshold for SCL and SDA. This permits its use in systems that use other than TTL voltages. The switching (threshold) voltage may be set from 0.5v to 3.0v. The default value is 1.5v.

To set the threshold voltage go to the I²C option screen (See Figure 5), press the ▼ on the ALD-232A-I2C. This will move the selection arrow down to the threshold voltage line. Use the ◀ and the ▶ until the desired voltage appears [in the range of 0.5v to 3.0v]. The selection will be saved for the next power up if either 5 seconds pass or if the **enter** key is depressed.

I2C	
MESSAGE #	0
IDLE	
->Threshold	1.5V

Figure 5 – Setting the threshold voltage

4.2. Run Time Display

When the analysis probe is running an I²C measurement, the unit's display will show the following information (See Figure 6):

I2C	
MESSAGE #	nnnnn
WRITING	aaa
->Threshold	1.5V

Figure 6 – I²C display during run

The second display line will denote the number of frames received. The MESSAGE # will show the counts (nnnnn) from 0 to 65536. The third display line shows the most recent frame's address (aaa) and if it was READ or WRITE transfer. On the fourth line the 1.5V on the display line indicates the threshold voltage that was set (or default if not explicitly set).

4.3. Logic Analyzer Connections

The ALD-232A-I2C supports simultaneous state and timing analysis. POD 1 is used for state analysis and POD 3 is for timing. For state analysis, the analysis probe accumulates the serial data and presents it to the logic analyzer as bytes along with some control signals on POD 1. The signals on POD 3 are buffered versions of SDA and SCL, the same control signals from POD 1 repeated and a 10-bit address is provided by the analysis probe after decoding the address byte(s).

The organization of these signals is shown in Tables 2 and 3 below.

POD 1 channel	Signal
8:0	Data Byte + ACK bit
9	FRAME
10	Read/Write*
11	START
12	STOP
clk	podClk

Table 2 – Pod 1 signals

POD 3 channel	Signal
9:0	Address
10	SCL I ² C clock
11	SDA I ² C data
12	Read/Write*
13	START
14	STOP
clk	podClk

Table 3 – Pod 3 signals

4.4. State Analysis

When configured for state analysis using state filtered.xml the overview configuration of the analyzer is shown. If state.xml is used then the Filter/Colorize-1 Tool will be missing.

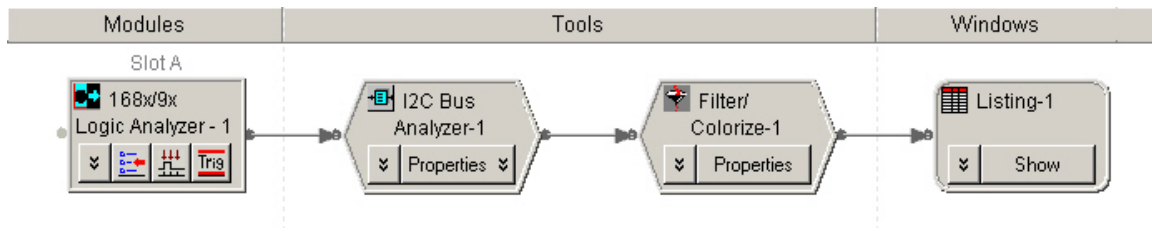


Figure 7: State Configuration Overview

Notice that between the analyzer module and the listing window, there are two tools. The first, the I²C Bus Analyzer-1 [a.k.a. data formatter] is the tool that formats the data on the screen of the analyzer. This tool allows the user to set the color of each type of I²C byte by selecting the Properties as shown below.

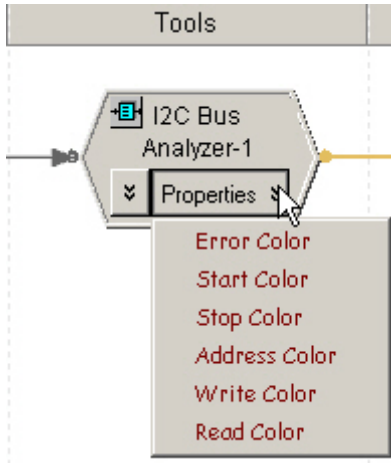


Figure 8: I2C Inverse Assembler Properties

The next tool is the standard Agilent Filter/Colorize tool. This can be used to selectively display or hide certain data types. It is not required in state.xml, but is used in state filtered.xml. It does not change the format of any displayed line, only whether that line is displayed or hidden.

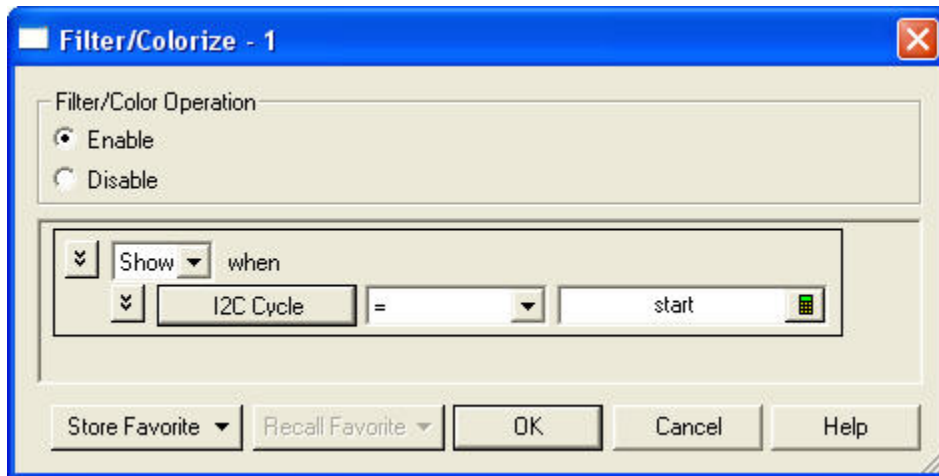


Figure 9: Filter Dialog Box

The state display in state DATA.xml shows 6 columns as shown in Figure 10. This configuration contains some I²C data so it can be seen how it is to be displayed. The configuration must be loaded “OFFLINE”. Load the state.xml file when you are ready to capture data from the DUT. The first is merely a sequence number. Notice that all of the captured lines are present (non-filtered). The second column, **I2CAddr** looks

suspiciously like column 5, **ADDR**. Column 5 is provided by the I²C analysis probe hardware and therefore cannot determine the I²C address until it has been sent, thus it is delayed until after the address byte is received. The field **I2CAddr** is provided by the Inverse Assembler (data formatter) software. It is not so restricted and therefore is able to display the correct I²C address from the START flag through the STOP flag of the message. [**ADDR** can be used in the triggering and filtering sequence, whereas **I2CAddr** cannot.]

The third column, **I2C CYCLE**, displays each byte captured and interprets that byte. The fourth column, **I2C Message**, is simply a repeat of the data in the following **I2C CYCLE** entries until the end of message (STOP). Thus if a user wanted to save screen space and didn't care about the details, he could use the filter to only display the START cycles and suppress the other columns. This is shown in the filtered display in Figure 11.

This filtered display is provided in configuration **state filtered DATA.xml**. It can only be viewed "OFFLINE". This is what the captured data of the I²C bus should look like.

Number	I2CAddr	I2C Cycle	I2C Message	ADDR	Time
-15	00A3	FLAG START	S A3 R 0D NAK P	0A2	345.000 us
-14	00A3	ADDRESS A3h		0A2	99.748 us
-13	00A3	Read 0Dh NAK		0A3	453.992 us
-12	00A3	FLAG STOP		0A3	185.152 us
-11	00A2	FLAG START	S A2 W 00 0C P	0A3	358.396 us
-10	00A2	ADDRESS A2h		0A3	99.752 us
M1 -9	00A2	Write 00h		0A2	257.992 us
-8	00A2	Write 0Ch		0A2	217.78 us
-7	00A2	FLAG STOP		0A2	213.616 us
-6	007F	FLAG START	S 7F R FF NAK P	0A2	257.872 us
-5	007F	ADDRESS 7Fh		0A2	99.784 us
-4	007F	Read FFh NAK		07F	537.736 us
-3	007F	FLAG STOP		07F	185.152 us
-2	004D	FLAG START	S 4D R FF FF FF FF NAK P	07F	350.024 us
-1	004D	ADDRESS 4Dh		07F	99.748 us
M2 0	004D	Read FFh		04D	340.088 us
1	004D	Read FFh		04D	226.152 us
2	004D	Read FFh		04D	234.556 us
M2 3	004D	Read FFh NAK		04D	415.46 us
4	004D	FLAG STOP		04D	185.124 us
5	009E	FLAG START	S 9E W 40 1C P	04D	484.02 us
6	009E	ADDRESS 9Eh		04D	99.812 us
7	009E	Write 40h		09E	257.964 us
8	009E	Write 1Ch		09E	217.776 us
9	009E	FLAG STOP		09E	213.62 us
10	00A2	FLAG START	S A2 W 02	09E	299.744 us
11	00A2	ADDRESS A2h		09E	99.78 us
12	00A2	Write 02h		0A2	257.996 us
13	00A3	FLAG START	S A3 R 09 NAK P	0A2	345.836 us
14	00A3	ADDRESS A3h		0A2	99.78 us
15	00A3	Read 09h NAK		0A3	453.988 us
16	00A3	FLAG STOP		0A3	185.152 us
17	0074	FLAG START	S 74 W 00 FC FC 60 DA P	0A3	1.58131 ms
18	0074	ADDRESS 74h		0A3	99.784 us
19	0074	Write 00h		074	257.964 us
20	0074	Write FCh		074	217.808 us
21	0074	Write FCh		074	217.776 us
22	0074	Write 60h		074	217.772 us
23	0074	Write 00h		074	217.78 us

Figure 10: Unfiltered State Display

umber	I2C Addr		I2C Message	Time
-15	00A3	S	A3 R 0D NAK P	703.612 us
-11	00A2	S	Created by I2C Inverse Assembler - 1	1.09729 ms
-6	007F	S	I2C Address	1.04701 ms
-2	004D	S	4D R FF FF FF FF NAK P	1.1727 ms
5	009E	S	9E W 40 1C P	1.98515 ms
10	00A2	S	A2 W 02	1.08892 ms
M1 → 13	00A3	S	A3 R 09 NAK P	703.612 us
17	0074	S	74 W 00 FC FC 60 DA P	2.32023 ms
25	0076	S	76 W 01 02 7D 6F 02 P	2.56314 ms
33	00A2	S	A2 W 07 85 P	1.7674 ms
38	00A2	S	A2 W 00	157.422 ms
41	00A3	S	A3 R 0D NAK P	703.58 us
45	00A2	S	A2 W 00 0C P	1.09732 ms
50	007F	S	7F R FF NAK P	1.04701 ms
M2 → 54	004D	S	4D R FF FF FF FF NAK P	1.1727 ms
61	009E	S	9E W 40 1D P	1.98515 ms
66	00A2	S	A2 W 02	1.08892 ms
69	00A3	S	A3 R 09 NAK P	703.612 us
73	0074	S	74 W 00 FC FC 60 DA P	2.32024 ms
81	0076	S	76 W 01 02 7D 6F 02 P	2.56314 ms
89	00A2	S	A2 W 07 85 P	1.76737 ms
94	00A2	S	A2 W 00	149.609 ms
97	00A3	S	A3 R 0D NAK P	703.58 us
101	00A2	S	A2 W 00 0C P	1.09729 ms
106	007F	S	7F R FF NAK P	1.04704 ms
110	004D	S	4D R FF FF FF FF NAK P	1.17266 ms
117	009E	S	9E W 40 1E P	1.98518 ms
122	00A2	S	A2 W 02	1.08892 ms
125	00A3	S	A3 R 10 NAK P	703.612 us
129	00A2	S	A2 W 01	1.08892 ms
132	00A3	S	A3 R 15 10 12 00 NAK P	703.608 us
139	0074	S	74 W 00 FD FC 60 DA P	3.4929 ms
147	0076	S	76 W 01 02 48 7D 02 P	2.56314 ms
155	00A2	S	A2 W 07 85 P	1.76737 ms
160	00A2	S	A2 W 00	154.456 ms
163	00A3	S	A3 R 0D NAK P	703.58 us
167	00A2	S	A2 W 00 0C P	1.09729 ms
172	007F	S	7F R FF NAK P	1.04704 ms
176	004D	S	4D R FF FF FF FF NAK P	1.17267 ms

Figure 11: Filtered State Display

The user may also specify symbols for the I2CAddr addresses to make the display more readable. Select **Setup|Symbols** from the menu of the logic analyzer and the Symbols dialog box, shown in Figure 12 will be displayed.

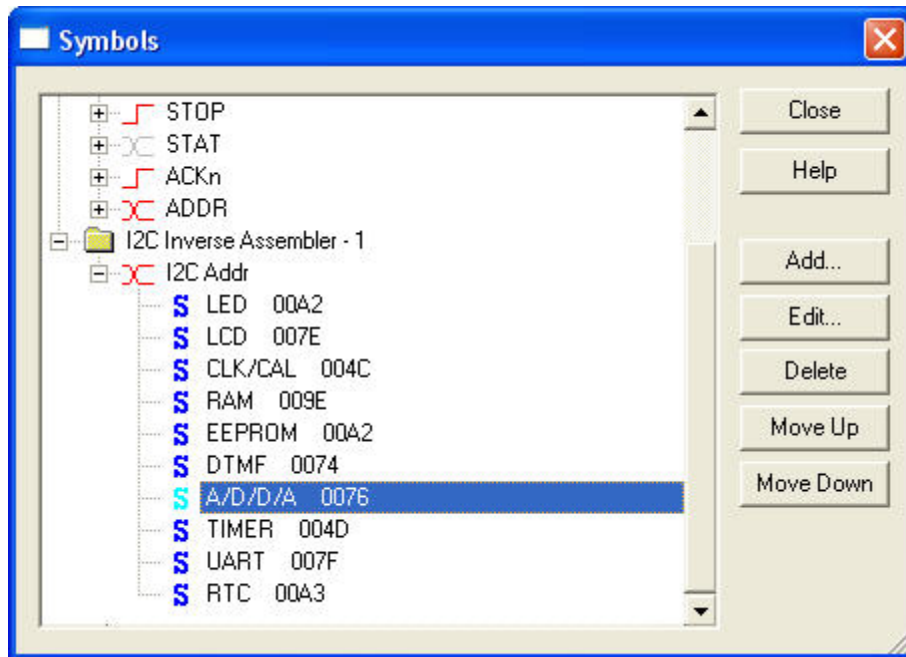


Figure 12: Symbols Dialog Box

Entering the symbols shown above would produce the following display in the listing window:

umber	I2C Addr		I2C Message	Time
-15	RTC	S	A3 R 0D NAK P	703.612 us
-11	LED	S	A2 W 00 0C P	1.09729 ms
-6	UART	S	7F R FF NAK P	1.04701 ms
M1 → -2	TIMER	S	4D R FF FF FF FF NAK P	1.1727 ms
5	RAM	S	9E W 40 1C P	1.98515 ms
10	LED	S	A2 W 02	1.08892 ms
M1 → 13	RTC	S	A3 R 09 NAK P	703.612 us
17	DTMF	S	74 W 00 FC FC 60 DA P	2.32023 ms
25	A/D/D/A	S	76 W 01 02 7D 6F 02 P	2.56314 ms
33	LED	S	A2 W 07 85 P	1.7674 ms
38	LED	S	A2 W 00	157.422 ms
41	RTC	S	A3 R 0D NAK P	703.58 us
45	LED	S	A2 W 00 0C P	1.09732 ms
50	UART	S	7F R FF NAK P	1.04701 ms
M2 → 54	TIMER	S	4D R FF FF FF FF NAK P	1.1727 ms
61	RAM	S	9E W 40 1D P	1.98515 ms
66	LED	S	A2 W 02	1.08892 ms
69	RTC	S	A3 R 09 NAK P	703.612 us
73	DTMF	S	74 W 00 FC FC 60 DA P	2.32024 ms
81	A/D/D/A	S	76 W 01 02 7D 6F 02 P	2.56314 ms
89	LED	S	A2 W 07 85 P	1.76737 ms
94	LED	S	A2 W 00	149.609 ms
97	RTC	S	A3 R 0D NAK P	703.58 us
101	LED	S	A2 W 00 0C P	1.09729 ms
106	UART	S	7F R FF NAK P	1.04704 ms
110	TIMER	S	4D R FF FF FF FF NAK P	1.17266 ms
117	RAM	S	9E W 40 1E P	1.98518 ms
122	LED	S	A2 W 02	1.08892 ms
125	RTC	S	A3 R 10 NAK P	703.612 us
129	LED	S	A2 W 01	1.08892 ms
132	RTC	S	A3 R 15 10 12 00 NAK P	703.608 us
139	DTMF	S	74 W 00 FD FC 60 DA P	3.4929 ms
147	A/D/D/A	S	76 W 01 02 48 7D 02 P	2.56314 ms
155	LED	S	A2 W 07 85 P	1.76737 ms
160	LED	S	A2 W 00	154.456 ms
163	RTC	S	A3 R 0D NAK P	703.58 us
167	LED	S	A2 W 00 0C P	1.09729 ms
172	UART	S	7F R FF NAK P	1.04704 ms
176	TIMER	S	4D R FF FF FF FF NAK P	1.17267 ms

Figure 13: Filtered Listing with User Symbols

4.5. Timing Analysis

SDA and SCL are presented to the logic analyzer on Pod 3 and may be used to view the signal timing. In addition to the two basic bus signals, the analysis probe also provides some additional signals that assist the timing display (see Figure 14).

The analysis probe will capture the I²C address after detecting the start event and will provide this as a 10-bit field that can be displayed with the timing. Note that this field cannot be accurate until after the 1st or 2nd byte of the frame (depending upon the address

mode). In addition to the address, the type of transfer, read or write, is also provided for the timing display, but with the same validity restriction

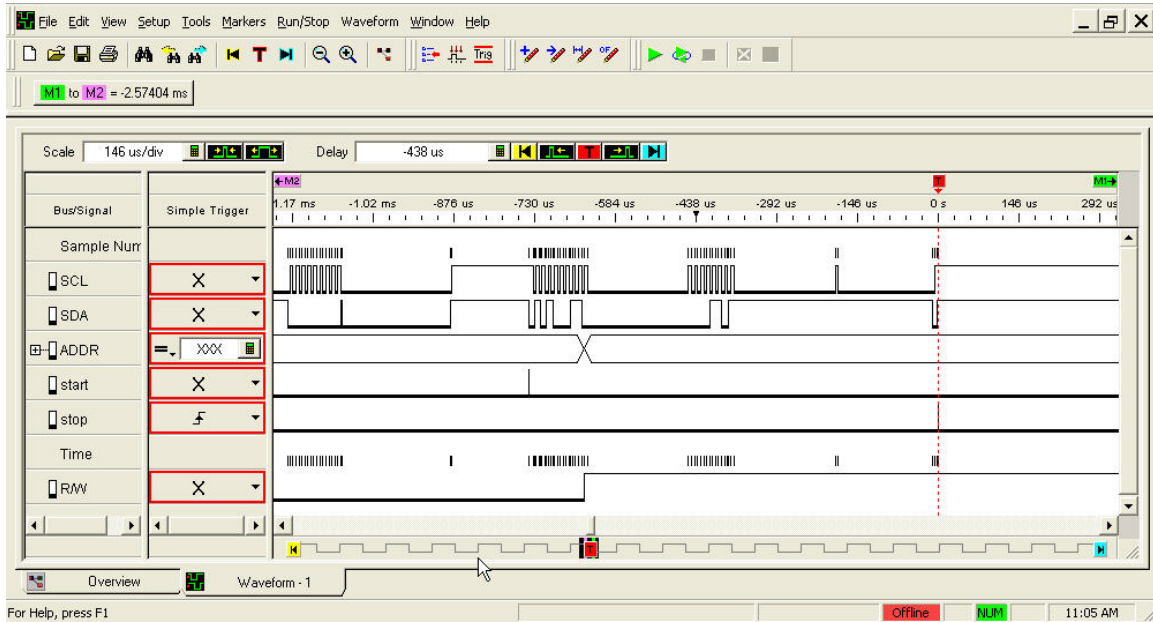


Figure 14 – Timing display

In addition, separate pulses are generated by the analysis probe identifying the start and stop events and at each byte boundary to assist in timing interpretation. The screen shot illustrates some of the timing features.

SCL and SDA displayed in timing mode have been delayed from the probed inputs. This happens as a result of passing through the adjustable input comparator and a buffer. This is not serious since the skew between SDA and SCL is, worst case, less than 10 ns and this is far less than the specified rise and fall times (300 ns.). The only time one should keep this in mind is when probing other signals in conjunction with the I²C bus.

5. Theory of Operation

The block diagram of the ALD-232A-I2C analysis probe is shown below (See Figure 17):

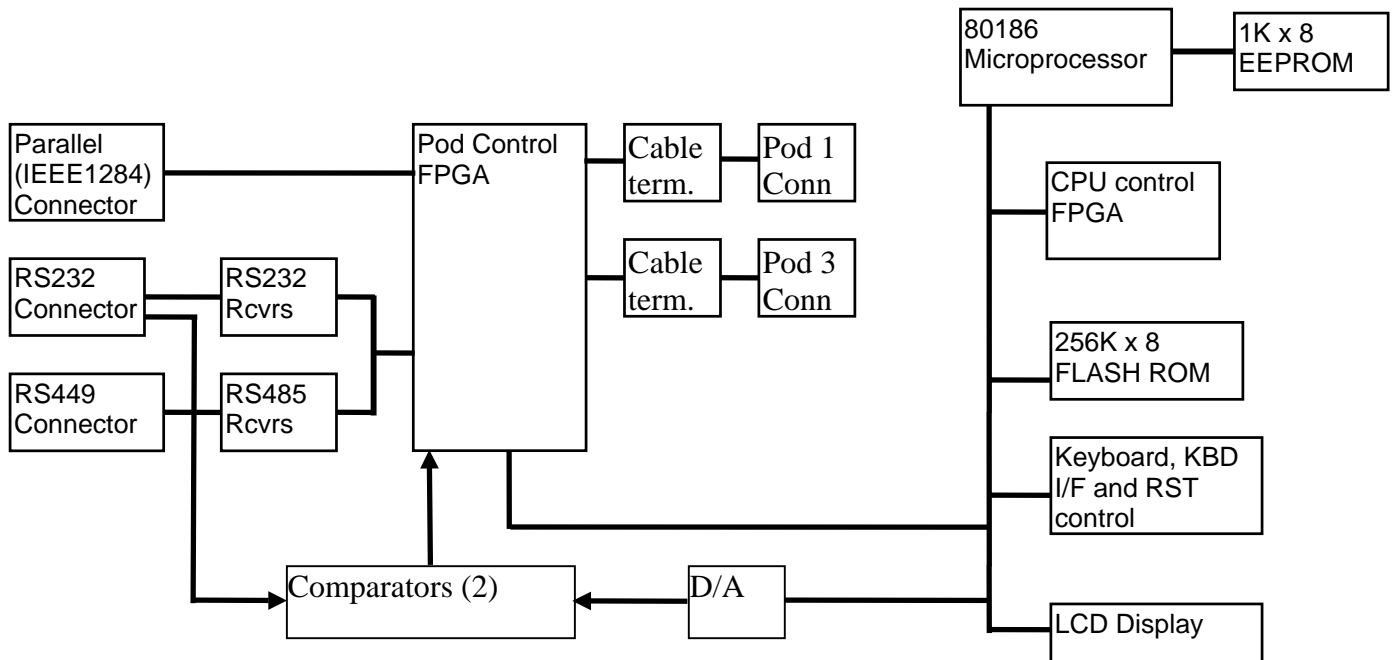


Figure 15 – Diagram of operation

The ALD-232A-I2C is a complete small processor system, with RAM, ROM, keyboard and display and a data capture system. The microprocessor system downloads the FPGAs with code appropriate to the operation selected, and receives parametric data from the user to program both FPGAs

The 80186-microprocessor system is conventional in design with the processor running at 32 MHz. Each time that the user selects a new parameter or option, that selection is recorded in the EEPROM. Data is also stored in the EEPROM after any mode change persists for more than 5 secs. This allows that selection to survive power loss. The Flash PROM contains not only the operational code, but also binary images of the code in both FPGAs. The CPU Control FPGA is downloaded automatically from the FPROP prior to the release of RESET from the 186. The Pod Control FPGA is downloaded under program control with code for RS232, RS449, IEEE1284 or I²C or any option that may be included.

The Pod Control FPGA collects data from the appropriate interface, RS232, RS449, IEEE1284 or and presents it to the pins of the logic analyzer. The FPGA acts as a dual UART or USRT for serial modes and an I²C receiver for that bus.

In I²C mode, the SDA and SCL inputs are connected via the RS232 (J2) port to 2 comparators, whose reference voltage has been set from a D/A converter on the microprocessor bus. This is the user selectable threshold voltage. After level detection, they are sent to the Pod Control FPGA. This FPGA contains all of the necessary logic to process the I²C signals, START and STOP detection, address detection, serial to parallel converter, etc.

The FPGA directly generates the signals that are sent to the logic analyzer's Pod 1 and Pod 3.

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