

**USER GUIDE**  
**SPI OPTION**  
**FOR THE ALD-232A**  
**BUS ANALYSIS PROBE**  
**(For Agilent 1680/90/800/900)**



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## 1. Introduction

The SPI option for the ALD-232A-SPI analysis probe allows users to examine the operation of an SPI bus without having to manually decipher the serial protocol for the bus. The ALD-232A-SPI analysis probe will display the data on the bus in an easy to read two column format.

### 1.1. Specifications

- Bus Loading: 20k $\Omega$  shunted by 30 pF (at probe tip)
- Probe Cable length: 15 in
- Connectors: female 0.025" square post
- Power Required: ~325 mA supplied by the logic analyzer
- Mechanical: 4.0" x 7.5" x 2.0"
- Signals supported: MOSI, MISO, CLK, and CS
- Skew: skew due to signal buffering less than 10ns
- Bus Speed: 8 MHz max CLK

### 1.2. Features

- SPI bus serial information is displayed as parallel words in state mode
- Quickly determine the information content of SPI transactions
- View details of SPI bus timing with signal pass-through mode
- View transactions in state mode using time tags, or in timing mode or both
- Operates non-invasively in real-time at speeds to 8MHz
- Preprocessor display shows snapshots of both MOSI and MISO
- Save measurement setup time with predefined configuration software for the logic analyzer
- Does not require termination adapters
- Includes all of the features of the ALD-232A Analysis Probe (RS232, RS449, and IEEE1284)
- Word lengths configurable from 1 to 32 bits per word.
- Data and chip select polarities configurable
- Operation with and without chip select is supported
- Several clocking options available

### 1.3. Logic Analyzers Supported

The SPI bus analysis probe may be used with all currently available 1680/90, 16800/900-series logic analyzers. Only two 17-channel pods are required.

## 1.4. Installing the Software

A CDROM is supplied with the SPI option for 1680/90/800/900 analyzers. Insert the CD into the drive in the analyzer. Click on the START menu and select RUN. When the RUN dialog box appears, click '**Browse**' and navigate to the CD. Select '**Installation Files\SPI\setup.exe**' and then click '**Run**'. This will start the installation process. Click NEXT on each screen until the final screen, then click FINISH.

**NOTE: Revision 3.x or later must be installed from Agilent before opening the configurations**

This will install the data formatter program used for displaying the data from the SPI pod. It will also install two configuration and two data files in the default directory structure for the logic analyzer. It creates the directory and files below:

C:\Documents and Settings\[user name]\My Documents\Agilent Technologies\Logic Analyzer\Config Files\SPI

SPIsetup.xml.	This configuration provides SPI setup only
SPI+data.xml	SPI configuration with DATA
SPI+data01of02.mfb	SPI DATA file
SPI+data02of02.mfb	SPI DATA file

**Note: .xml Configuration with "DATA" in the title contain captured data and can be used for demonstration purposes. They must be viewed "OFFLINE".**

## 1.5. Equipment Supplied

- RS232D, RS449, and IEEE 1284 and SPI Bus Analysis Probe
- This User Guide
- An ALD232A User Guide for the 16700 series analyzer
- Diskettes with configuration files and screen data formatter for the 16700 family for the basic ALD-232A serial and parallel options
- CDROM with configuration and data formatter files for the 1680/90 and manuals for all of the ALD-232A options
- 2 flat ribbon 'Y' Cable for connecting to the target bus for RS232, RS449 and IEEE1284
- SPI attachment cable

## 1.6. Minimum Equipment Required

In addition to the equipment supplied above, an Agilent 1680/90/800/900 logic analyzer is required.

## **2. Installation**

The ALD-232A-SPI is easy to install. The unit is simply connected between the logic analyzer and the SPI target and the supplied configuration is loaded into the logic analyzer.

### ***2.1. Initial Inspection***

Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until the contents of the shipment have been inspected mechanically and electrically. If the contents are incomplete, if there is mechanical damage or defect, or if the instrument does not operate, notify Advanced Logical Design, Inc. If the shipping container is damaged, or the cushioning materials show signs of stress, notify the carrier as well as the ALD office. Keep the shipping materials for inspection by the carrier.

### ***2.2. Connection to the Logic Analyzer***

The ALD-232A-SPI derives its power from the logic analyzer and provides data through the pod connection cables. Both pods 1 and 3 should be connected. Pod 1 provides state data and Pod 3 provides timing data. Note that Pod 2 is not used. The pod cables from the logic analyzer are plugged directly into the right side of the ALD-232A. No additional terminators or adapters are required.

### ***2.3. Connection to the Bus***

The ALD-232A-SPI has several connectors on the top of the unit that allow it to be attached to several busses. The connector used for the SPI bus is the one identified as J1. The LED adjacent to J1 will be lit when the SPI option is selected. A short cable is supplied with a mating 26 pin IDC connector on one end and the other has 7 individual wires, terminated with sockets intended to connect to 0.025" square posts. These can be hooked directly to wirewrap posts on the unit under test or may be used with the grabbers supplied with the logic analyzer.

There are 4 SPI signals, clock, chip select, MOSI (Master Out Slave In) data and MISO (Master In Slave Out) data. These are connected to the unit under test from the supplied cable as shown in Table 1 below:

Cable Wire	J1 Pin	Function
purple	17	SPI Chip Sel (CS)
gray	18	Gnd
white	19	SPI CLK
black	20	Gnd
brown	21	MOSI (Master Out Slave In)
red	22	Gnd
orange	23	MISO (Master In Slave Out)

**Table 1 – SPI cable signals**

## 2.4. Loading The Configuration

There are two configuration files for the ALD-232A-SPI. Both files include simultaneous state and timing analysis. The first file:

SPIsetup.xml

will load the configuration with no data in the buffer. This file is to be used when capturing data. The other file:

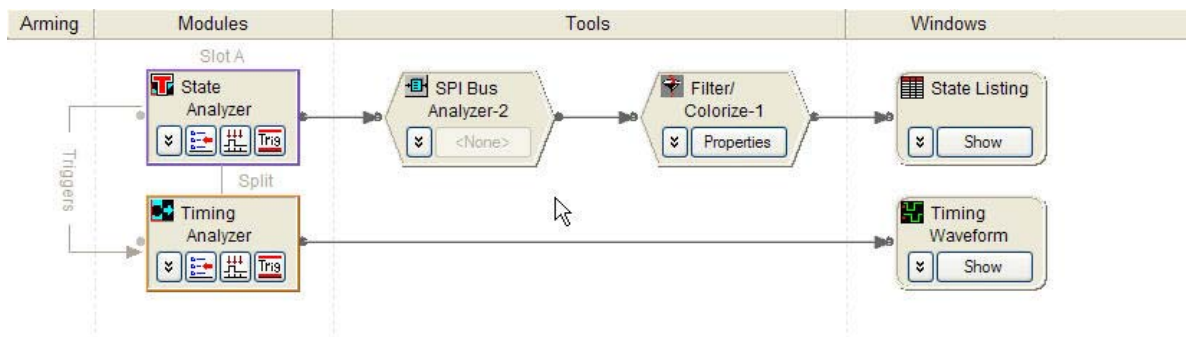
SPI+data.xml

calls 2 additional data files that contain example data:

SPI+data01of02.mfb and SPI+data02of02.mfb.

The SPI+data.xml file needs to be loaded 'Offline' to be able to load the saved data. This can be used to become familiar with the 'Filter/Colorize-1' tool and display format.

Both configurations splits the analyzer into a state and a timing analyzer as shown below:

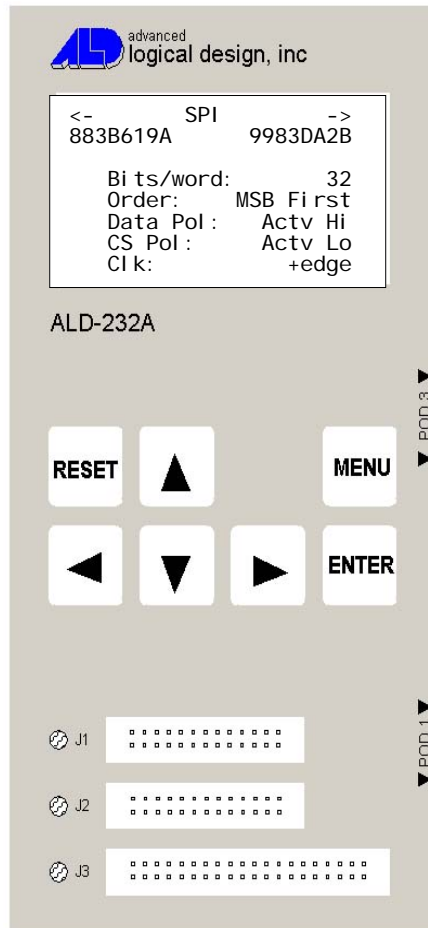


**Figure 1: SPI Analyzer Overview**

### 3. Operational Overview

Immediately after power is applied or **RESET** is depressed, the ALD-232A-SPI will enter self-test mode. After the self-test is completed, the ALD-232A-SPI will enter the RUN mode, with the interface connection (J1, J2 or J3) that was last used. The LED opposite the appropriate connector (J1) will be lit.

All operations of the ALD-232A are controlled by the keyboard (See Figure 1). When the logic analyzer cables are plugged into the ALD-232A, the unit will power up in the mode it was last in. Navigation through the options is very simple. An arrow (->) will point to the item that can be changed. A new value may be selected for that item by scrolling through the choices with the ◀ and the ▶ keys. To move to a different item, use the ▲ and ▼ keys. The item at the top of the screen is the type of analysis desired [RS232 ASYNC, RS232 SYNC, RS449 ASYNC, RS449 SYNC, IEEE 1284 and SPI]. The last screen in the sequence is an informational screen.



**Figure 2: ALD-232A-SPI top panel**

The operation of the ALD-232A-SPI in modes other than SPI is explained in the basic ALD-232A manual, also enclosed. This addendum covers only the SPI operation.

## 4. Analyzing SPI

The SPI (Serial Peripheral Bus) does not have an industry standard specification. A minimum implementation uses 3 signals; clock and 2 data lines. It is a full duplex bus, meaning that data travels in both directions, from master to slave and slave to master. This accounts for the signal naming:

Clock  
MOSI (Master Out Slave In)  
MISO (Master In Slave Out)

It is very common that a chip select (CS) is also used when multiple slaves exist on the same bus. Bus speeds may run for a few KHz to over 10 MHz. The ALD-232A-SPI will operate at speeds up to 8 MHz.

Beyond these general outlines, the details are left to the implementer. The ALD-232A-SPI supports the following parameters:

Bits per word: 1 to 32 bits per word  
Bit Order: MSB or LSB first  
Data Polarity: either high or low  
Chip Select Polarity: either high, low or not used  
Clock: data valid on either the positive or negative going edge

These parameters are set using the controls on the front panel of the ALD-232A.

### 4.1. Run Time Display

When the analysis probe is running an SPI measurement, the unit's display will show the following information (See Figure 3):

```
<-      SPI      ->
883B619A      9983DA2B

Bi ts/word:      32
Order:      MSB First
Data Pol :      Actv Hi
CS Pol :      Actv Lo
Cl k:      +edge
```

**Figure 3 – SPI display during run**

The first line indicates that the SPI mode is in operation. The 2 hex numbers on the second line are snapshot values of recent MOSI (left) and MISO (right) data. The remainder of the screen indicates the selected parameters for the bus. These may be changed and using the ▲ and ▼ keys to select the parameter and then using the ◀ and the ▶ keys to select the desired value.

## 4.2. Logic Analyzer Connections

The ALD-232A-SPI supports simultaneous state and timing analysis. POD 1 is used for state analysis and POD 3 is for timing. For state analysis, the analysis probe accumulates the serial data and presents it to the logic analyzer as bytes along with some control signals on POD 1. Since word lengths can exceed 8 bits, and both MOSI and MISO data must be sent to the logic analyzer, multiple transactions are necessary to provide all of the data to the logic analyzer. This is accomplished on Pod 1. Pod 3 is not multiplexed and contains real time data used on the timing side.

The organization of these signals is shown in Tables 5 and 6 below.

POD 1 channel	Signal
7:0	Data
12:8	Code (used to provide parametric data to the analyzer software)
14:13	Not used
15	Flag (used to identify the first transaction in the series)
clk	podClk

**Table 2 – Pod 1 signals**

POD 3 channel	Signal
0	MOSI
1	MISO
2	CS
3	Pod 1 clk *
4	MOSIi*
5	Clk33*
6	Frame*
7	Clki*
15:8	Spi
clk	SCLK

**Table 3 – Pod 3 signals**

\* These are internal signals and are not generally valuable to the user.

MOSI, MISO, CS and SCLK are buffered versions of the user's SPI input and are used for timing analysis.

## 4.3. State Analysis

The state display is shown in Figure 4 below. An 8 bit per word data size was selected in this example. A 32 bit per word state display is shown in Figure 5. Notice that the sample number column entries are missing entries. This is because the preprocessor must send several samples to the logic analyzer to provide all of the required data. The analyzer presents the accumulated data on the first sample line in the data series. The other lines are suppressed by the Filter/Colorizer tool. The signal on Pod 1, channel 15, Ald1st, is the flag that identifies this sample and is used by the Filter/Colorizer.

Sample Number	MOSI	MISO	Time
0	78	87	0 s
2	F1	0E	2.244 us
4	EF	10	4.500 us
6	0B	F4	6.748 us
8	78	87	41.248 us
10	F1	0E	43.496 us
12	EF	10	45.744 us
14	0B	F4	48.000 us
16	78	87	82.496 us
18	F1	0E	84.748 us
20	EF	10	86.996 us
22	0B	F4	89.248 us
24	78	87	123.748 us
26	F1	0E	125.996 us
28	EF	10	128.248 us
30	0B	F4	130.496 us

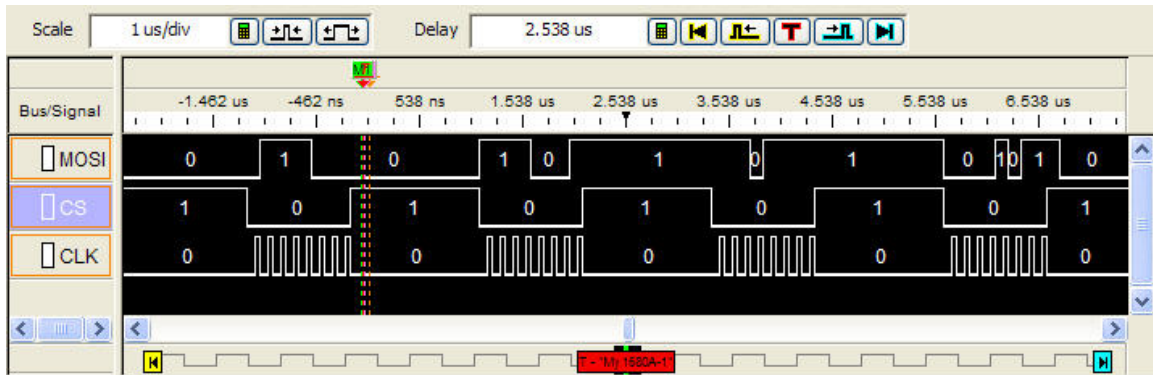
Figure 4: 8 bits/word, State Display

Sample Number	MOSI	MISO	Time
0	1234 5678	EDCB A987	0 s
8	9ABC DEF1	6543 210E	5.252 us
16	DEAD BEEF	2152 4110	10.504 us
24	ADEA DBOB	5215 24F4	15.752 us
32	1234 5678	EDCB A987	53.248 us
40	9ABC DEF1	6543 210E	58.500 us
48	DEAD BEEF	2152 4110	63.752 us
56	ADEA DBOB	5215 24F4	69.000 us
64	1234 5678	EDCB A987	106.500 us
72	9ABC DEF1	6543 210E	111.752 us
80	DEAD BEEF	2152 4110	117.000 us
88	ADEA DBOB	5215 24F4	122.252 us
96	1234 5678	EDCB A987	159.748 us
104	9ABC DEF1	6543 210E	165.000 us

Figure 5: 32 bits/word, State Display



In Figure 7 an active low chip select was chosen. Four discrete 8 bit words are sent and are framed by CS [low]. If CS is not used, the above situation couldn't work since there is no way to distinguish the end of one word and the beginning of the next. This situation is shown in Figure 8.



**Figure 8: 8 bits/word, Blocked Clock**

In this figure, the SCLK is only active when the data is active. Data is aligned into words by counting the correct number of clocks. If this type of operation is chosen, it is important that SCLK is idle when the option is selected, otherwise it is unknown where the ALD-232A-SPI will start counting [it is unlikely to be correct].

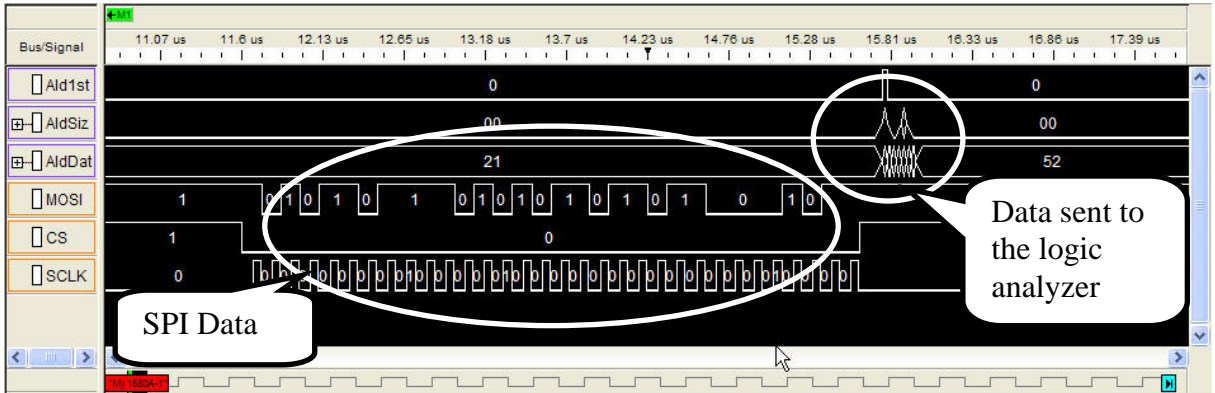
Chip select may also be used in the above case, in which case the idle clock precaution is not necessary since the data is properly framed by CS.

#### **4.6. SPI Data / Logic Analyzer Protocol**

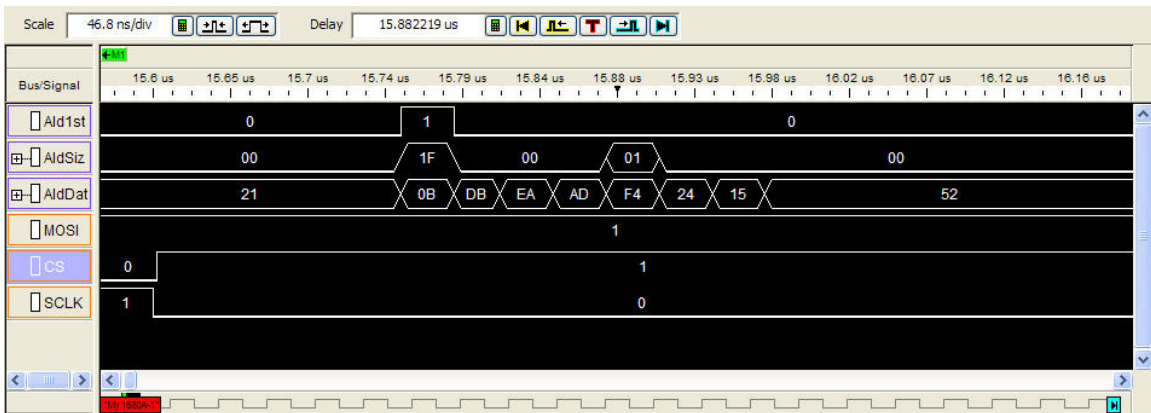
While it is not absolutely necessary to understand the data flow between the logic analyzer and the ALD-232A-SPI, it might help in some situations.

As mentioned above, not all of the data needed by the logic analyzer can be sent in one clock since up to 64 bits of user data (MOSI and MISO) as well as several bits of control information are needed on a single, 17 channel, pod. The required data is sent serially after the last data bit has been received.

Figure 9 shows the relationship of the SPI and logic analyzer data. The 64 bits of SPI data (32 bits MOSI and 32 bits MISO) and control data is sent in an 8 clock [max] burst after the trailing edge of CS. The logic analyzer clock is 32 MHz. This burst is expanded in Figure 10.



**Figure 9: SPI and Logic Analyzer Data**

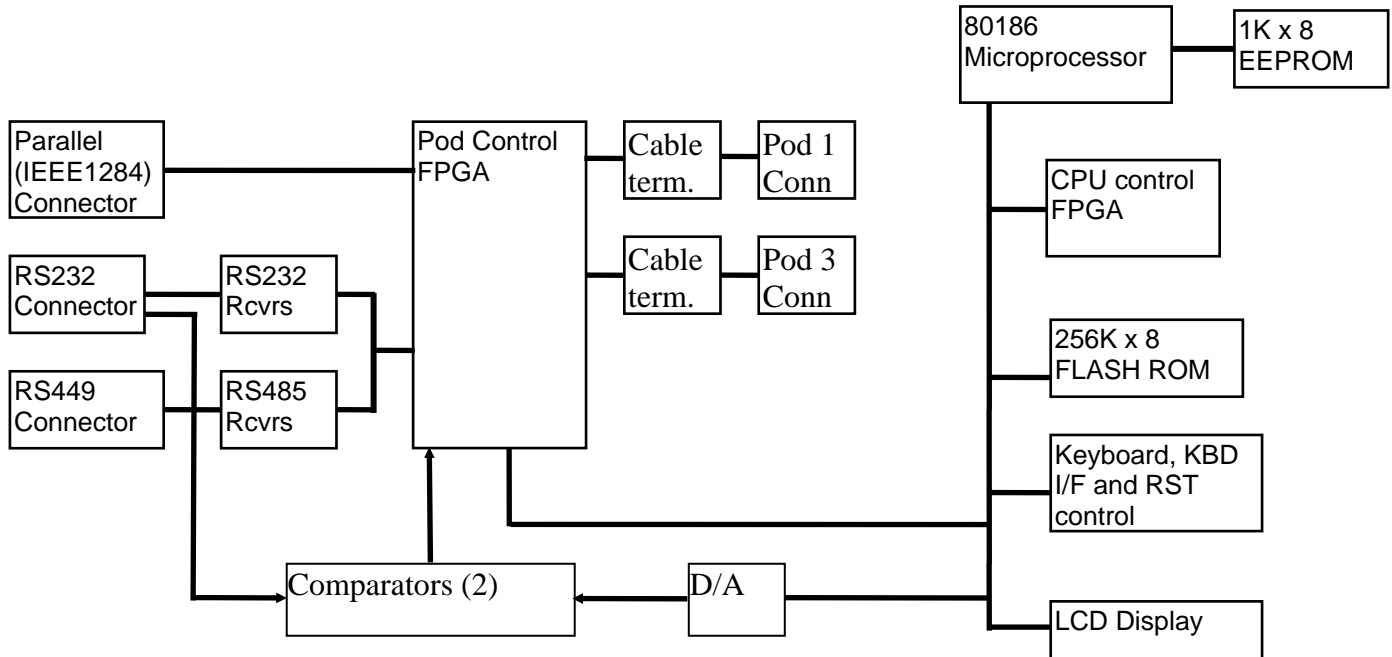


**Figure 10: Expanded Logic Analyzer Burst**

The burst of data to the logic analyzer illustrated in Figure 10 [32 bits per word] shows 8 blocks of data with fields AldDat, AldSiz, and Ald1st. The AldDat field contains 8, 8 bit bytes with the MOSI and MISO data. Ald1st is a flag that identifies the first block of data. AldSiz contains the number of bits/word – 1 during the first block and the bit order during the 4<sup>th</sup> block [for 32 bits/word].

## 5. Theory of Operation

The block diagram of the ALD-232A-SPI analysis probe is shown below (See Figure 11):



**Figure 11 – Diagram of operation**

The ALD-232A-SPI is a complete small processor system, with RAM, ROM, keyboard and display and a data capture system. The microprocessor system downloads the FPGAs with code appropriate to the operation selected, and receives parametric data from the user to program both FPGAs

The 80186-microprocessor system is conventional in design with the processor running at 32 MHz. Each time that the user selects a new parameter or option, that selection is recorded in the EEPROM. Data is also stored in the EEPROM after any mode change persists for more than 5 secs. This allows that selection to survive power loss. The Flash PROM contains not only the operational code, but also binary images of the code in both FPGAs. The CPU Control FPGA is downloaded automatically from the FPRM prior to the release of RESET from the 186. The Pod Control FPGA is downloaded under program control with code for RS232, RS449, IEEE1284 or SPI or any option that may be included.

The Pod Control FPGA collects data from the appropriate interface, RS232, RS449, IEEE1284, or SPI and presents it to the pins of the logic analyzer. The FPGA acts as dual shift registers for MISO and MOSI data and an output mux to send the data to the logic analyzer.

The FPGA directly generates the signals that are sent to the logic analyzer's Pod 1 and Pod 3.

Rev A

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